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Development of Prototype RF Front-End Electronics For Linear Accelerator Beam Position Monitoring System

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ABSTRACT

DEVELOPMENT OF PROTOTYPE RF FRONT-END ELECTRONICS FOR LINEAR ACCELERATOR BEAM POSITION MONITORING SYSTEM

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Beam position monitoring (BPM) systems are utilized extensively in particle accelerator facilities as a diagnostic tool to ascertain quantitative aspects of an accelerated charge beam such as spatial position and intensity of the beam as it is accelerated to greater velocities and levels of kinetic energy within said accelerating machine. A critical aspect of a BPM system is the radio frequency front end (RFFE) electronic circuitry that receives the incoming raw BPM signal and performs signal conditioning such that its frequency spectrum is transformed from radio frequency (RF) to non-RF and digitization of the transformed signal by downstream components can successfully occur. While front-end implementations such as RF heterodyne receivers or peak detectors are commonly used to transform the incoming signal into digitizable form, a front-end implementation is proposed and investigated in this study that utilizes a three-stage active filter consisting of a bipolar junction transistor in common emitter configuration to amplify the incoming signal and a standard LC bandpass filter to filter and elongate it so that digitization of it by downstream sample-and-hold (SAH) and analog-to-digital converter (ADC) components can successfully occur.
DEVELOPMENT OF PROTOTYPE RF FRONT-END ELECTRONICS FOR LINEAR ACCELERATOR BEAM POSITION MONITORING SYSTEM

BY

EDWARD SIEBERT

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A THESIS SUBMITTED TO THE GRADUATE SCHOOL

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Thesis Director:

Dr Mansour Tahernezhadi
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DEDICATION

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CHAPTER 1

INTRODUCTION

Section 1.1: Problem Statement

Beam position monitoring (BPM) systems play an important diagnostic role in the activity of monitoring beam charges as they are accelerated within a particle accelerator. As the beam of charged particles is accelerated within the accelerator to speeds near to the speed of light, an accompanying amount of kinetic beam energy on the order of millions of electron volts can also be achieved. Contingent upon this outcome is the proper monitoring of the charge beam with respect to its spatial position as it is being accelerated through the particle accelerator. It is the primary role of a BPM system to extrapolate this position information via electrode sensors placed within the accelerator walls that can electrically detect the accelerated beam as it passes by. An essential accompanying component is an RF front end (RFFE) that interfaces with the electrode sensor to condition the incoming signal (which is induced on the electrode pickup via electric fields from the accelerated beam of charged particles passing it by) so that it can be successfully digitized by downstream analog-to-digital hardware components. Once digitization of the signal occurs, then position information of the beam at that specific location within the accelerator beampipe can afterward be derived.
An imposing dilemma in this realm of endeavor is related to properly detecting the incoming BPM signal in view of its extremely narrow pulse width which can typically lie between 200 and 800 picoseconds. Although ultra-high-bandwidth oscilloscopes exist, in most scenarios the cost to purchase them and use as a direct way of measuring the incoming raw BPM signal (that typically originates from four separate electrode pickups) can be prohibitively high. It is therefore more economical for an RF front end (RFFE) circuit to be designed so that it conditions and transforms the BPM raw incoming RF signal in such a way that its essential features are linearly retained but in a frequency range that is compatible with the bandwidths of the sample-and-hold and analog-to-digital components which typically are not in the RF range.

Moreover, recent efforts have been made by the Argonne Wakefield Accelerator (AWA) facility in Lemont, Illinois to develop the front-end electronics for a prototype BMP system that they would like to design and deploy on the linear accelerator that they have at their facility [1]. For the purposes of this study, I am a participant in the Chicagoland Accelerator Science Traineeship (CAST) program, funded by a grant of the United States Department of Energy, so as to work collaboratively with local particle accelerator facilities partnering with CAST and to design and test accelerator science-based prototype systems that can be utilized at their facilities. The budget and resources at AWA are limited in scope, so they are seeking to design a BPM prototype RFFE for the linear accelerator at their facility, the electronics of which is low cost to design and implement. Concomitant to this outcome is the objective of meeting the performance and system requirements of the linear accelerator at their facility with respect to the range of beam charge levels the accelerator can produce as well as the run-time attributes of the charge beam itself.
Section 1.2: Research Question

A vital aspect of the proposed BPM prototype RFFE electronics is to condition the incoming BPM signal such that it can properly fit within the frequency bandwidth of the sample-and-hold and/or analog-to-digital hardware components. For this to successfully occur, the frequency spectrum of the incoming signal must be altered in such a way that the signal’s bandwidth lies within the bandwidth of the sample-and-hold and/or analog-to-digital hardware components. This invariably leads to some method whereby the width of the incoming BPM signal is elongated in time. Therefore, the primary research question of this study is whether the RFFE electronics for a BPM system can be designed for AWA facility such that the full range of beam charge (i.e. 1pC to 100nC) is properly detected by the RFFE while it simultaneously elongates the width of the incoming BPM raw signal to such a degree that the peak amplitude of resulting elongated signal can be uniquely mapped to the peak amplitude of input signal and digitized utilizing a low-cost sample-and-hold circuit.

Section 1.3: Hypothesis

It is hypothesized to propose a low-cost method for conditioning the incoming BPM signal in the RFFE board so that digitization of its peak amplitude can successfully occur. It is to employ
a three-stage active filter utilizing BJT transistors in common emitter configuration for amplification of the incoming BPM signal and a second-order LC bandpass filter to remove the high-frequency contents of the signal and (thereby elongate it) such that digitization of it can occur.

This will require that the active filter in both amplification and filtering (of the incoming signal) operates in a linear fashion and range so that its output response (in terms of peak amplitude) is always in direct proportion to the peak amplitude of the incoming unfiltered BPM signal. When this condition is met, the position information of the accelerated beam can be later extrapolated in a manner that is predictable and secure.
A survey of existing literature on BPM systems, specifically as it relates to the electronics of the RFFE, reveals that there are several different ways that signal conditioning of the incoming raw BPM signal occurs. In all cases, the purpose of the front-end electronics is to primarily transform the incoming signal from having a radio frequency (RF) band to a lower intermediate-frequency (IF) band (or to a base-band frequency band) so that digitization of the signal can afterward occur. The main different ways in which this transformation of frequency spectrum occurs (as seen in the surveyed literature) is either by demodulation of the signal (via a RF mixer and local oscillator), elongating the signal via an envelope and/or peak detector circuit, utilizing third-party off-the-shelf electronic circuit packages specifically designed for the RFFE of BPM system, or avoiding the use of front-end electronics and signal conditioning by routing the raw incoming BPM signal directly into ultra-high-bandwidth oscilloscope-based equipment.

In [2] and [3], the RFFE consisted mainly of attenuators and/or amplifiers that conditioned the incoming BPM signal before having it directly digitized by RF analog-to-digital converters in the several-GHz range. The signals were then processed further in either the time or frequency domain to extract pertinent information related to the amplitude and/or phase of the incoming BPM signal so that position information from it could be derived. In the case of [3], additional computations were done in the frequency domain of the digitized signal so that adjustment of aliasing from under-sampling could occur and the corresponding impulse response of the BPM
signal could afterward be successfully reconstructed. After equalization of the signal was done in the frequency domain, then the inverse Fourier transform was applied to the signal’s spectrum so that a corresponding reconstruction of the incoming signal in the time domain could be obtained [3].

In [4] and [5], the method of direct sampling is employed to digitize the incoming BPM raw signal in its original form without transforming its frequency spectrum. The main reason this method succeeds is due to the high sampling rates (1 GHz or higher) that the oscilloscopes in [4] and [5] have to digitize in the raw incoming BPM signal. The oscilloscopes have to be manually configured by human operators in order to intercept the incoming BPM raw signals each time a new and separate charge beam needs to be detected. Depending on the pulse width of the incoming raw signal, this form of implementation can be especially cost prohibitive, especially due to the fact that four separate oscilloscopes are needed to accurately extrapolate the vertical and horizontal positions of the detected particle beam. For the case of the BPM prototype system as proposed in this study, the incoming raw BPM signal has a pulse width of approximately 400 picoseconds. After doing initial research into the cost of third-party oscilloscope equipment that can accurately digitize the raw BPM signal, and due to its prohibitively high purchasing cost, this method of RFFE implementation cannot not be seriously considered as a viable method to pursue.

In [6] the RFFE implementation of a BPM system largely consists of utilizing a third-party off-the-shelf hardware and software product specifically designed for beam instrumentation systems as used in particle accelerator facilities. The name of the hardware module is Libera Brilliance Single Pass and is designed by Instrumentation Technologies. In [6], in order for the RFFE of the BPM system to properly interface with the Libera module, the incoming raw BPM
signal into the RFFE board had to be down-converted to the operating frequency of the Libera unit, which was 500 MHz. For the purposes of the BPM signal detector (i.e. RFFE) board as proposed in this study and the pulse width of the raw BPM signal incoming to it, a similar implementation as described in [6] would not be a viable option to pursue in that a significant amount of signal conditioning would need to be done to the raw incoming signal before the remainder of the front-end work could be accomplished via the Libera Brilliance board. From a perspective such as this, utilizing the Libera unit as part of the RFFE would therefore be serving a self-defeating purpose.

In [7] an approach to measuring beam position information was done by measuring the phase difference between two BPM-induced raw signals as they propagated down two separate coaxial transmission lines. The RFFE in [7] consisted mainly of a grounded coplanar waveguide transmission line and a reflectometer to which the electrode pickups of the BPM-induced signals are connected. The transmission lines in the reflectometer are able to detect any phase mismatch between incoming signals. If the charge beam is not centered between two electrode pickups, the time it takes for each induced signal to reach the end of each transmission line will then be different, and the reflectometer will be able to detect and measure this difference in phase between the two induced BPM signals. From this computation of phase difference between the two transmitted signals, the position information of the beam can then be extrapolated. Due to the direct computation of phase mismatch between the incoming BPM signals as they propagate on two separate transmission lines, the method as proposed in [7] does not require digitization of the raw BPM signal so as to extrapolate beam position information via downstream digital front-end components. Unfortunately though, the beam aperture of [7] by design has to be rectangular in
shape and is not compatible with the aperture at AWA lab, which is circular in shape. Therefore a front-end design, as proposed in [7], cannot be considered in this study as a viable option to pursue.

In [8], the RFFE to the proposed BPM system consisted essentially of a peak detector with Schottky diode to condition the incoming raw BPM signal and trace out its amplitude envelope. The incoming raw BPM signal into the RFFE is first low-pass filtered and then passes through a series of attenuators and low-noise amplifiers to either attenuate or amplify it based on the charge level of the beam that induced it. The RFFE was designed to detect incoming BPM signals having as low as a 30pC charge level. Use of a peak detector then elongated the signal and in doing so removed its higher frequency components and transformed it into a non-RF signal. The output of the peak detector was then digitized using an analog-to-digital converter on a separate digital front-end board. As a salient feature, a delay line and broadband combiner are used to serially route two raw BPM signals, as received from two separate BPM electrode pickups into one RFFE board [8].

To further enhance its performance, the RFFE electronics in [8] were expanded in [9] to include several new features. In particular, the functionality of the peak detector circuitry was enhanced by using an anti-parallel Schottky diode to improve the sensitivity of detecting the input signal. Furthermore, there was an upgrade from two to four separate RF input channels on the RFFE board, which permits it to now have two separate BPMs connected to it at the same time. Each RF input channel was expanded to receive data from two separate BPM pickups that are combined in quadrature into one signal by delaying the incoming BPM signal from one of the pickups before the signals are combined and fed into a single RF input channel on the RFFE board. The use of a peak detector implementation was also investigated early on at the AWA facility but it was deemed unsuitable to utilize for the RFFE board due to the fact that it had a reverse-bias
parasitic capacitance that allowed the high-frequency components of the BPM raw signal to pass through it while in cutoff mode. Moreover, the non-linear behavior of the diode in the near-to-conduct 0.7V range meant that a peak detector implementation for the BPM prototype RFFE board would not be considered further at the present time [9].

In [10] the RFFE of the BPM system utilized two separate diode-based peak detectors that were used to condition and elongate the incoming raw BPM signals from the two electrode pickups. The output of each peak detector was then fed into a high-impedance differential amplifier to output the difference between the peak amplitudes of the two BPM signals. The signal then passed through bandpass and bandstop filters to improve the dynamic range of the signal. Digitization of the signal then occurred via an analog-to-digital converter. For the same reasons as stated in [8, 9], the diode implementation in [10] was not considered due to its use of a diode-based implementation.

In [11], there are several factors in the design of the BPM RFFE system that are worth noting. One salient feature is that RFFE utilizes a third-party component to perform the signal conditioning operations on the raw incoming BPM signal. An RF envelope detector chip (model ADL5511) by Analog Devices was utilized to output the envelope of the incoming signal so that it can afterwards be digitized by downstream digital front-end components. The ADL5511 chip is able to operate on an input frequency range from DC up to 6 GHz. For the BPM system of [11], the RF frequency of the Booster Synchrotron accelerator is 31.6 MHz. The usage of the ADL551 chip reduces the complexity of the RFFE design and therefore presents itself as a viable choice for implementing the signal conditioning aspects of the RFFE. It was later discovered that the ADL551 envelope detector chip is suitable only for continuous-wave (CW) RF input signals. Since
the input to the BPM prototype RFFE board is a pulsed RF signal, the RFFE implementation as described in [11] cannot be further considered.

One salient feature of the RFFE design in [11] is that a low-noise pre-amplifier is mounted directly on the BPM electrode pickup itself so as to immediately amplify the BPM signal before it propagates down the BNC cable that is attached to the electrode pickup. In so doing, the signal-to-noise ratio of the BPM signal is greatly improved in that its magnitude envelope can be increased. This is done in the presence of any other sources of noise that are superimposed over it as the BPM signal propagates through the BNC cable and/or other downstream RFFE elements that may make contributions to the magnitude of the noise floor of the RFFE board.

Another noteworthy aspect of the RFFE design in [11] was the use of a free simulation tool by Analog Devices to measure the noise and/or distortion effects of interconnected RF components such as low-noise amplifiers, attenuators, mixers and/or bandpass filters. The simulation tool, named ADIsimRF, can be used to plot simulation data in graphical form related to tradeoffs in system design between performance of the interconnected components and any undesirable after-effects such as increased distortion or noise figure of the input signal in the RF chain of components being simulated [11, 12]. This feature will therefore be further explored and possibly used in the future if components from Analog Devices are utilized for the BPM prototype RFFE board (or are considered for utilization) so that their performance attributes can be further analyzed.

In [13] the RFFE for the BPM system computed both the amplitude and phase of a single-bunch beam being detected. A heterodyne detector was then employed in the RFFE to shift the frequency spectrum down from radio frequency (RF) to intermediate frequency (IF) range such
that it fit within the frequency bandwidth of downstream digitization components. After
digitization of the entire BPM signal envelope, in-phase and quadrature (i.e. I and Q) data were
extracted from the signal via down-sampling so that position and phase information of the single-
bunch particle beam (as detected by the RFFE) could be obtained. The in-phase and quadrature
sampling is needed due to the fact that the phase of the incoming BPM signals is not known in
advance, and only the bunching frequency of the beam bunches is known as they enter the RFFE
board. The I and Q sampling method allows the peak amplitude of each bunch to be calculated
based on the I and Q samples of the signal that are made at the same rate as the bunching frequency
of the beam bunches as they arrive [14].

In [15], an RFFE was designed for a single-shot accelerator having BPM strip-line pickups.
The signal conditioning was done in parallel for each BPM signal from strip-line pickup. As such,
the RFFE first bandpass filtered the raw incoming BPM signal with a center frequency of 2.856
GHz, which is the RF frequency of the particle accelerator. The signal is then down-converted
using an RF mixer to center frequency of 350MHz. A low-pass filter than removes any unwanted
signals outside of the IF bandwidth, which is 3.5MHz. This bandwidth is established by surface
acoustic wave (SAW) bandpass filters. All filters, attenuators and amplifiers in the signal
conditioning path are impedance matched to each other so as to reduce signal losses at their
respective inputs and outputs. The signals from each pickup are then fed into a 180-degree ring-
hybrid network so that the position information of the beam can be ascertained. The output of the
hybrid network is then digitized using ADC components.

In [16], the RFFE design utilizes a heterodyne mixer to down-convert the incoming BPM
signal from RF to IF form. As in other heterodyne receiver paradigms examined above, the
incoming signal is first low-pass filtered to remove unwanted frequency components of the BPM signal before any mixing operations are performed. Variable attenuators are then used to allow the incoming signal to have a wider dynamic range. The local oscillator (LO) frequency of the heterodyne mixer is actually generated from a RF signal coming from the particle accelerator itself and is then mixed using a phase-lock-loop (PLL) hardware component. After the signal is down-converted to an IF range (via the heterodyne mixer), the entire signal is digitized. In-phase and quadrature base-band data (corresponding to amplitude and phase of the BPM signal) is then extracted via demodulation from the BPM signal now in digital form [16].

In contrast to the heterodyning procedures previously seen in RFFEs surveyed here, the RFFE in [17] employed a self-homodyne mixer to directly translate the incoming BPM signal (in RF form) down to base-band form. After the signal is mixed down to a base-band frequency range, it is low-pass filtered, amplified, and then digitized by downstream sample-and-hold and analog-to-digital converter components on the digital front-end board that is adjacent to it.

For the RFFE implementations described in [13, 15-17] above, a heterodyne or homodyne mixer was used to down-convert a high-frequency signal to either intermediate or base-band range. The frequency of the signal that is down-converted via the heterodyne mixer is typically in the immediate range of the RF frequency of the particle accelerator itself and typically is the frequency component that contains the most energy when analyzing the various frequency components of the signal in the frequency domain. Due to the need for having additional components such as local oscillators, phase-lock-loop, and voltage-controlled oscillators, this type of design can be more costly and complicated to implement, especially in the case of asynchronous pulsed-RF input signals. For this reason, the heterodyne or homodyne mixing method of RFFE
implementation was not pursued when choosing a design paradigm to implement for the BPM prototype RFFE system at the AWA facility.

In [18], an incoming BPM signal to the RFFE is first bandpass filtered using a surface acoustic wave (SAW) filter. Then the signal is attenuated and/or amplified to fit it within the input range of the ADC converter. The entire envelope of the signal is then bandpass sampled (and thereby down-converted to IF range) via digitization by an ADC converter. The down-converted signal is then demodulated to in-phase and quadrature (I and Q) base-band form via a FPGA-based digital down-converter (DDC) and finite impulse response (FIR) filter [18]. The RFFE of this implementation is similar to that of the BPM prototype RFFE in that the input signal is amplified and elongated (via bandpass filtering) before digitization of it occurs. A difference is that the center frequency of the bandpass filter in [18] is at the RF frequency (508MHz) of the particle accelerator itself, whereas with the BPM prototype RFFE board, the center frequency is at 1.59MHz, which permits the elongated signal at the output of the corresponding filter to lie immediately within the 3dB bandwidth of the sample-and-hold circuit on the BPM signal processing board. Moreover the entire envelope of the signal in [18] is digitized, whereas for the BPM prototype RFFE board, only the peak amplitude of the elongated signal is digitized.
CHAPTER 3

BPM THEORY OF OPERATION

Section 3.1: Physics of Particle Accelerator

The acceleration of charged particles within a particle accelerator is accomplished by the electromagnetic forces that are applied to them in a strategic and systematic manner. The electromagnetic force itself is the superposition of an electric force, which interacts with the charged particles via an electric field, and a magnetic force, which interacts with the charged particles via a magnetic field. The direction of the electric force is always parallel to the direction of the electric field that generates it, and the direction of the magnetic force is always orthogonal to the direction of the magnetic field that generates it. Because the vectoral components of acceleration are proportional to the vectoral components of force, the electric force affects both the energy and trajectory of the charged particles, whereas the magnetic force affects only the trajectory of the charged particles. As a result of this, strategically placed magnets are used within a particle accelerator to change the trajectory of particles being accelerated, and high-voltage oscillators are used to change the kinetic energy of particles being accelerated [19].

Due to the fact that only the electric force can be in parallel with a charged particle’s direction of motion, it only can do work on a charged particle and increase its momentum and kinetic energy. Designers of particle accelerators therefore utilize electric fields to initiate and
sustain the acceleration of charged particles until a desired level of kinetic energy and/or momentum of the particles is achieved [19].

As seen in Figure 1, one means by which a particle accelerator initiates the acceleration of a charged particle is via the photoelectric effect. In a typical scenario, a light source (usually a laser) is projected onto a cathode material in such a way that the energy transported by the light matches one of the energy levels of the electrons that are bound to the atoms in the cathode material. When this match in energy occurs, the light incident on the cathode causes electrons to be emitted from the cathode due to the energy that is being provided to it via the photons in the radiated light. When the electron is ejected from the material, it’s free to move in the presence of an applied electric field. An alternating voltage source is also attached to the cathode such that when an electron is ejected from the cathode material, it is immediately swept up under the electric field, the polarity of which causes it to be accelerated away from the cathode material to which it was previously bound (subatomically) [20].
For linear particle accelerators, the general way in which charged particles are accelerated is via an external oscillating RF voltage source that is connected to the accelerator itself. For half of every cycle of the oscillating RF voltage source, the corresponding electric force (as governed by the underlying electric field that is present in the RF voltage source) is parallel to the direction of motion the charge particles are traveling in. For the other half of each cycle of the RF voltage source, the direction of the corresponding electric force (as governed by the underlying electric field of the RF voltage source) is anti-parallel to the direction that the charged particles are traveling in. The oscillation of polarity in the RF source is exploited such that the charged particles travel through insulated drift tubes (and are shielded from the electric field of the RF voltage source) when the direction of the force is opposite to the direction the charged particles are moving in, and the charge particles are only exposed to the electric field (of the RF voltage source) when the direction of the force is parallel to and in the direction of their motion [21].

For linear particle accelerators, a typical manner in which the charged particles are shielded from the electric field is via insulating drift tubes within the accelerator that allow the charged particles to travel through them at constant velocity when the electric field of the oscillating RF voltage source is in opposition to their direction of motion. In this scenario, there is no net force on the beam of particles and they simply travel through the drift tubes at previous speed. Gaps between adjacent drift-tubes exist at the places where the polarity of the RF voltage source reverses, and the electric field (of the oscillating RF voltage source) points in the opposite direction to the direction of motion for accelerated particles that are negatively charged. In this manner, then, the charged particles are accelerated and acquire an increase in velocity and kinetic energy.
The physical length of each successive drift tube is longer to account for the greater distance that the accelerated charged particle travels in the same amount of time as it coasts through the adjacent drift tube while shielded from the opposing electric field of the oscillating RF voltage source. As illustrated in Figure 2, as the charged particles exit the adjacent drift tube, the polarity of the RF voltage source reverses again, and the charged particles are again exposed to the corresponding electric field that’s now parallel to their direction of motion and experience an additional increase in acceleration and kinetic energy [21].

![Diagram of Linear Accelerator and Oscillating RF Voltage Source](image)

Figure 2: Linear accelerator and oscillating RF voltage source [22].
For particle accelerators, typically the attribute of greatest importance pertaining to an accelerated charge beam is the amount of kinetic energy that it has. Between any two adjacent drift tubes, the change in kinetic energy is equivalent to the total amount of work done on the charge beam by the electric field as the charge beam moves between the gap of adjacent drift tubes. For charge beams moving at non-relativistic speeds, the increase in kinetic energy through all upstream drift tubes is [20]:

$$W_{total} = \Delta E_{total} = \frac{1}{2}mv^2$$

where:

$m = mass\ of\ the\ charge-beam$

$v = velocity\ of\ the\ charge-beam$

For charge beams moving at relativistic speeds, the total kinetic energy obtained from all upstream drift tubes is [20]:

$$W_{total} = \Delta E_{total} = \frac{mc^2}{\sqrt{1- \frac{v^2}{c^2}}} - mc^2$$

where:

$m = mass\ of\ the\ charge-beam$

$v = velocity\ of\ the\ charge-beam,\ c = velocity\ of\ light\ in\ vacuum$
For circular particle accelerators such as the *cyclotron*, the manner in which charged particles are accelerated involves the interaction of both magnetic fields (which govern the magnetic force) and electric fields (which govern the electric force) upon the charged particles being accelerated within the accelerator [20]. Having an initial velocity and level of kinetic energy upon entering the circular region of the particle accelerator, the charged particles enter immediately into a uniform magnetic field that causes the direction of the charge beam’s velocity to constantly change such that it moves in a circular motion. As seen in Figure 3, the uniform magnetic field interacts with the charge particle in such a way that the direction of the resulting force on the particle beam is radial and toward to center of the circular ring, thus causing the particle beam to move in a circular pattern at constant speed. At certain locations within the circular structure of the accelerator, there are small gaps within it that cause the charged particles to interact with an electric field that is parallel to their direction of motion. This interaction with the electric field therefore exerts a force on the particles, causing them to receive a “kick” and accelerate forward. After the charge beam passes this gap, it again interacts with the uniform magnetic field, thus causing it to resume a circular pattern of motion, but now on a trajectory with a greater radius due to the radial force it experienced from the electric field while passing through the one of the gaps of the circular structure of the particle accelerator [20].
Another kind of circular accelerator is the synchrotron. This type of accelerator is different from the cyclotron in that the diameter that the charged particles traverse (inside it) is of fixed length. Charged particles are typically injected into the synchrotron externally by a linear accelerator. A linear accelerator first increases the kinetic energy and velocity of the particle beam to a specific threshold level and then injects the particle beam into the synchrotron so that its kinetic energy level and velocity can be further increased as the particle bunch circulates within its ring-like structure. Electromagnets that generate magnetic fields of varying magnitude are positioned within the storage ring to sustain the same orbit radius of the injected charge beam as it circulates around the storage ring of the synchrotron [21].

In a scenario of charge beam particles being accelerated to higher levels of energy or scenario of travelling at a plateau-level of steady-state energy, it’s critical that the center of mass of the particle beam be well maintained and kept spatially centered within the beam pipe of the particle accelerator. By maintaining its centeredness, the motion of the charge beam can be stabilized and kept from becoming oscillatory and/or unpredictable. This can primarily be done.
by using steering magnets and by having a way to monitor the spatial position of the particle beam in a non-invasive manner at various points while it travels within the particle accelerator. A beam position monitoring (BPM) system is the primary means by which position information of the beam can be extrapolated and obtained. The BPM system consists of electrode pickups embedded within the accelerator itself, RF front-end electronics to condition and transform the induced raw signal from the electrode plates, and an interconnected digital front-end system that digitizes the conditioned BPM signal and extrapolates from it the position of the beam. After position information of the beam becomes known, either a human operator or closed-loop feedback system connected to the BPM system can make corrective adjustments to the beam’s trajectory towards centeredness via steering magnets that are embedded within the particle accelerator.

Section 3.2: BPM Electrode Pickup

A beam position monitoring electrode pickup functions as the gateway through which a BPM signal is created/induced and fed into the BPM prototype RFFE board via a coaxial transmission line. As an electrical sensing device, and as seen in Figure 4 below, the BPM electrode pickup is embedded within the particle accelerator itself and electrically insulated from the wall of the accelerator beam pipe is able to detect when an accelerated beam of charged particles passes by it. This is accomplished by it functioning as a capacitor plate and responding to the changing electric fields of the beam of charged particles as it passes by it while being accelerated. Based on Maxwell’s equations, a displacement current is created between the BPM
electrode pickup and the beam of charged particles (during the time it is in the immediate vicinity of the BPM pickup) due to the charge beam’s varying electric fields that the electrode pickup is able to detect [23].

The relative magnitude of the induced voltage from the BPM electrode pickup is in proportion to the net charge of the particle beam and its spatial proximity to the electrode pickup itself. The basic envelope of the induced voltage from the electrode pickup remains unchanged (for beams with a Gaussian current profile, it is the first derivative of a Gaussian charge distribution), but it is scaled by how close the particle beam is to the BPM electrode pickup. Speaking generally, the charge level of a particle beam is in direct proportion to the sum of induced voltages on BPM button electrode plates that are parallel to one another. With respect to its spatial location however, the position of a particle beam is in direct proportion to the normalized difference between induced voltages on BPM button electrode plates that are parallel to one another [23].
Therefore, it is the relative distance that the charge beam is from each BPM electrode pickup that allows for its position to be extrapolated once the BPM incoming signal has been filtered and digitized with respect to its peak amplitude. This is based on the fact that when the particle beam is closer to an electrode pickup, a greater voltage will be induced on it than when it is farther away from an electrode pickup. A difference-over-sum normalization procedure can then afterward determine the position of the particle beam based on the difference in peak amplitudes of the BPM input signals as induced onto the four BPM electrode pickups by the charge beam as it passes by. The difference-over-sum formula can therefore be expressed as [24]:

\[
\begin{align*}
\gamma &= \frac{1}{S_y} \frac{V_{\text{up}} - V_{\text{down}}}{V_{\text{up}} + V_{\text{down}}} + \delta_y \\
\chi &= \frac{1}{S_x} \frac{V_{\text{right}} - V_{\text{left}}}{V_{\text{right}} + V_{\text{left}}} + \delta_x
\end{align*}
\]

where:
$V_{up}, V_{down}$ are the induced peak voltages on the upper/lower BPM pickup plates

$V_{right}, V_{left}$ are the induced peak voltages on the right/left BPM pickup plates

$S_x, S_y$ are horizontal/vertical proportionality constants

$\delta_x, \delta_y$ are BPM horizontal/vertical offset correction values

As illustrated in Figure 5, the BPM electrode pickup (and a coaxial cable attaching it to the BPM prototype RFFE board) can be modeled as a voltage source in series with a capacitor and load resistor where the output voltage is taken over the load resistor of the lumped-component model. As seen in the same figure, the capacitor of the lumped model represents the BPM electrode pickup and its capacitance, and the voltage source represents the changing electric field of the charge beam as it passes by the BPM electrode pickup and the source of displacement current through the capacitor of the corresponding lumped circuit model. The load resistor in the corresponding lumped model represents the input impedance of the BPM signal detector board as seen from the electrode pick up via the coaxial cable that functions as a transverse electro-magnetic transmission line [23]. The formula [24] used for computing the BPM current (which is proportional to the BPM voltage) is based on the dimensions of the button capacitor plates and the centroid position and intensity of the charge beam that induces a current onto it and is given by the formula:

$$I_{im}(t) = \frac{dQ_{im}(t)}{dt} = \frac{A}{2\pi al} \frac{dQ_{beam}(t)}{dt}$$

where:
\[
\frac{dQ_{beam}(t)}{dt} = \frac{1}{\beta c} \frac{dI_{beam}(t)}{dt}
\]

and:

\[Q_{im}(t) = \text{total 'image' charge}, \quad Q_{beam}(t) = \text{total 'beam' charge}\]

\[l = \text{length of radius}, \quad A = \text{area of button plate}\]

\[a = \text{radius of beam pipe}, \quad c = \text{speed of light}\]

\[\beta = \text{relativistic scaling factor}\]

Due to the high frequency contents contained within the BPM raw signal, the coaxial cable functions as an RF transmission line (having a characteristic-impedance of \(Z_0\)).

Figure 5: BPM button-pickup lumped-component circuit model [23, 24].

As illustrated in Figure 6, the transfer function for the BPM electrode pickup and cable is therefore a first-order high-pass filter, meaning that the voltage across the load resistor will contain
mainly the higher frequency components of the induced BPM input signal via the electrode button pickup. As seen in the same figure, the cutoff frequency of the high-pass filter is simply:

\[ f_{\text{cutoff}} = \frac{1}{2\pi R_L C_b} \]

where \( C_b \) is the capacitance between the electrode pickup and the beam-pipe wall [23]. Due to the high-frequency content of the induced BPM signal, the coaxial cable functions as a transmission line and as such, any mismatch in load input impedance with the characteristic impedance of the coaxial cable will result in signal reflections between the BPM electrode pickup and prototype RFFE board.

![Frequency response of BPM button pickup lumped-component circuit model](image)

**Figure 6**: Frequency response of BPM button pickup lumped-component circuit model [25].

After signal conditioning and digitization of the incoming BPM signal by the RFFE BPM components occur, the centroid position of a detected charge beam can be determined using a difference-over-sum algorithm. The difference-over-sum algorithm essentially removes the beam
intensity information of the beam charge that is common to both BPM signals as detected and transmitted by the BPM electrode pickups. The removal of this information is accomplished by normalizing the magnitude of each digitized BPM signal and then computing the difference in magnitude between the two normalized signals. A proportionality constant is also applied so that the position information derived from the sum-over-difference computation is properly scaled in accordance with any calibration-related adjustments that need to be made so as to fully extrapolate the position information of the detected beam [23].

As seen in Figure 7, a raw incoming signal from the BPM electrode pickup has a bipolar pulse width of approximately 600 picoseconds and a nominal peak amplitude voltage of approximately 1.1 millivolts which corresponds to a beam charge level of approximately 1 pico-coulomb. As seen in the same figure, the corresponding frequency response of the same BPM signal is broadband in nature and, as seen in the figure, has a peak frequency magnitude at approximately 1.5 GHz.
A calibration of beam charge levels to corresponding induced button pick up voltages was previously done at the AWA facility to determine the relationship between beam bunch charge level and the corresponding input voltage of an accelerated beam bunch as induced on the BPM button pickup electrodes [1]. To determine the charge level, an integrated current transformer (ICT) located within local proximity to the BPM button pickup was used to measure the charge level of the beam bunch, and a high-speed oscilloscope was used to measure the corresponding voltage as induced in each of the four separate BPM pickups. Before being sent to the oscilloscope, the four button pickup voltages were combined into one signal via the use of a RF coaxial combiner. A range of beam bunch charge levels were measured so as to determine their one-to-one mapping and linearity to the voltages they induced on the BPM pickup. As seen in Figure 8, a
mapping of charge level to voltage was then plotted and linearized using a least squares method. The lower limit to the charge level that could be measured by the ICT unit was approximately 1 pico-coulomb [1].

![Figure 8: Mapping of BPM charge level to button voltage [1].](image)

The charge magnitude of accelerated charge beams at the AWA facility can extend from approximately 1 pico-coulombs to near micro-coulomb range [25], so it is imperative the BPM electrode pickups have a sensitivity to properly transduce the range of aforementioned charge levels into voltage levels that accurately correspond to them. The peak amplitude of an induced BPM raw signal for a 1 pico-coulomb beam charge is approximately 3 millivolts [26]. Moreover, via the BPM electrode pickup, the FWHM pulse-width of an induced BPM voltage signal from a passing beam of accelerated charged particles is approximately 100 pico-seconds [25].
Section 3.3: BPM Multi-Stage Active Filter

The BPM multi-stage active filter serves as the RFFE of the BPM prototype circuit. The active filter performs the signal conditioning functions on the pulsed-RF incoming BPM signal so that it may afterward be digitized by downstream SAH and ADC components on the BPM signal processing board. To this end, it is crucial that the incoming raw BPM signal, which contains a high concentration of frequency components in the gigahertz range, be transformed to non-RF form by removing its upper frequency components so as to satisfy the frequency bandwidth requirements of the sample-and-hold circuit on the signal processing board. A by-product of the filtering operation is that the BPM signal at the output of the active filter becomes elongated and slowed-down so that the “tracking” and “hold” operations of the sample-and-hold circuit on it can successfully occur. It is also critical to amplify the incoming BPM signal prior to filtering it. Due to the fact that the frequency components lying within the resonant band of the filter are much lower in amplitude than the superposition of all other frequency components of the incoming signal combined, the magnitude of the filtered signal, unamplified, would be too small for the SAH component on the BPM signal processing board to detect, and more likely too close (or under) the noise-floor voltage threshold of the BPM prototype RFFE board.

Another vital function of the BPM bandpass active filter is to transform the raw incoming BPM signal from RF to non-RF form so that any parasitic effects on downstream components of the BPM signal processing board are eliminated or mitigated to a significant degree. For this to occur, it is critical that the incoming BPM signal be transformed from RF to non-RF form as soon as possible so that these-parasitic effects don’t induce forms of signal crosstalk between reactive
components on the BPM signal detector board. In the case of the BPM multi-stage active filter, it is important that the parasitic effects of the signal are mitigated by transforming it (via bandpass filtering) from RF to non-RF form during the first stage of the cascaded filter-chain.

As seen in Figure 9, the BPM multi-stage active filter on the BPM prototype RFFE board is three separate active filters that are cascaded together for the purpose of amplifying and filtering the incoming raw BPM signal. The amplifier portion of the active filter utilizes a common emitter configuration topology of bipolar junction transistor (BJT). The filter portion of the active filter on the BPM prototype RFFE board is a LC bandpass filter and is used as a resonator to generate a strong minimally damped response at the resonant frequency that effectively slows down the incoming BPM signal so that it can be transformed into non-RF form for downstream digitization and signaling hardware components on the BPM signal processing board. As will be described later in this study, the BPM prototype system (in lieu of a peak detector) utilizes a sample-and-hold circuit to track the elongated BPM signal and latch it at its peak value via a trigger timing circuit that is also on the BPM signal processing board.
It is important to note that for the active filter of the BPM prototype RFFE board, the envelope of the incoming raw BPM signal is not of interest but rather its peak amplitude alone. This is in contrast to other implementations as observed in some of the literature of BPM RFFE systems as surveyed in this study. In implementations such as those, the entire waveform of the incoming BPM signal, after signal conditioning, is digitized by downstream components and as such the integrity of the entire waveform is important to preserve. It is for this reason that the BPM signal processing board, as described in this paper, has timing and synchronization circuitry to only digitize the peak amplitude of the output signal of the BPM prototype RFFE board rather than its entire amplitude envelope.

Therefore, a main endeavor in designing the active-filter of the BPM prototype RFFE as proposed here is that the peak-amplitude at the filter output is in direct correspondence to the peak amplitude of the input signal to the active filter, either via a linear relationship or via a unique one-
to-one mapping between input and output. For the purposes of this study, only the centroid position information of the charge beam passing the pickup electrodes is of interest, and that information can be extrapolated from the peak amplitude of the incoming BPM signal which is in direct proportion to the distance of the charge beam from the BPM electrode plates [23].

As illustrated in Figure 10, a single-stage of the BPM active filter consists of an NPN transistor in common emitter configuration. As seen in the figure, the biasing resistor $R_e$ is the emitter-resistance, and the collector impedance $Z_c$ is frequency dependent and given by the expression:

$$Z_c = R_c + \left( j\omega L_{tank} || \frac{1}{j\omega C_{tank}} \right)$$

As seen in the figure, the $C_s$ and $C_c$ capacitors are used to prevent the DC-component current of the circuit (as supplied by $V_{cc}$, the 12-volt DC power supply) to flow into the BPM signal input (denoted by $V_s$, the voltage source) and into the next stages of the active filter. The capacitor $C_{bypass}$ functions as a bypass capacitor to provide a path to ground for any AC currents flowing from the DC power supply, and the $L_{choke}$ inductor (with a total resistance of 13Ω in the inductor’s coils) functions as a RF choke to prevent any high-frequency AC currents (from the BPM input signal denoted by the $V_s$ voltage source) from flowing into the 12-volt DC power supply.
Figure 10: BPM prototype multi-stage active filter (schematic diagram) [27].

The DC biasing of the active filter, as displayed in Figure 11, was done in such a way that the DC operating point for each stage of the active filter would be close to the upper part of the DC load line near the saturation level of the transistor. This was the desired place for the DC operating point to be so that the BJT transistor would conduct only on the negative portion of the incoming bipolar BPM signal, thus causing the LC resonator to produce a single output response at its resonant frequency. The DC biasing of the BJT transistor was therefore done by adjusting the values of the four bias resistors while comparing the output voltage of the transistor (from collector to ground) to the input voltage of the transistor (from base to ground) until such time that
the output voltage was slightly greater than that of the input voltage. Such a condition would therefore indicate that the DC operating point was just slightly outside the saturation region of the transistor but still relatively close to that point via the DC load line of the transistor.

![Diagram of DC-biasing configuration of BPM active filter (single stage) and DC load line and operating point](image)

Figure 11: a) DC-biasing configuration of BPM active filter (single stage) and b) DC load line and operating point [28].

The DC operating point, as seen in Figure 11, was computed in an anecdotal manner by connecting a 12-volt DC power supply to the BPM prototype RFFE board, turning it on, and then first determining the collector DC current (denoted as ‘I_c’ in part ‘a’ of Figure 11a) by using a multimeter to measure the DC voltage drop across the ‘R_c1’ resistor and then dividing it by the
resistance of the $R_{c1}$ resistor, which is 50 ohms. Using the same multimeter, the $'V_{CE}'$ DC voltage was then determined by simply adding up the measured voltage drop across the $'R_{c1}'$ resistor and $'R_{c2}'$ resistor (which represents the resistance in the coil of the active-filter LC resonator) and then subtracting from the total voltage drop the measured voltage drop across the $'R_E'$ resistor, as seen also in part ‘a’ of Figure 11a. For the DC load line analysis of the BPM RFFE board, the values of $'I_{c(sat)}'$ and $'V_{CE(cutoff)}'$ (as seen in part ‘b’ of Figure 11b) were computed by using the following DC load line formulas for BJT common-emitter transistors [28]:

$$I_{c(sat)} = \frac{V_{cc}}{R_C + R_E} = \frac{V_{cc}}{R_{C1} + R_{C2} + R_E}$$

$$V_{CE(cutoff)} = V_{cc}$$

The resonant frequency of the LC filter was chosen by monitoring the pulse width of the output waveform from the LC filter while exciting it with the raw BPM input signal. Specifically, the inductor component of the filter was given a fixed value and then the capacitance value of the capacitor was varied while examining the pulse width of the filter’s output response such that it was comparable to the bandwidth requirements of the sample-and-hold circuit on the BPM prototype RFFE board. The final values of the inductance and capacitance of the LC filter were then chosen, via the calibration process as described above, to be 1 milli-henry and 10 pico-farads. The center frequency $'f_c'$ (which is the resonant frequency) of the LC filter is then given by the equation:

$$f_c = \frac{1}{2\pi \sqrt{LC}} = \frac{1}{2\pi \sqrt{(1\times10^{-3})\times(10\times10^{-12})}} = 1.59 \text{Mhz}$$
The voltage gain of a single stage of the BPM active filter is directly proportional to the collector impedance of the biased BJT circuit [26]. Since the LC resonator is in the path of the collector current, the collector impedance is frequency dependent. This also implies that the voltage gain of a single stage of the active filter is frequency dependent as well. The impedance of an LC filter is always greatest at its resonant frequency, so its corresponding voltage output response, which is proportional to the filter’s impedance, will always be greatest at the resonant frequency as well.

The initial configuration of the active filter was initially as a single-stage transistor in common emitter configuration with a tuned LC filter attached to it for producing an elongated output response at the resonant frequency of the active filter. Initial simulation tests in LTspice by Analog Devices Corporation, using a nominal incoming BPM signal, indicated that a single-stage active filter could produce an output response of satisfactory peak magnitude. However, it was later discovered that the simulation results were not done under steady-state conditions of the prototype RFFE board and that it was instead operating in a “powered-up” transient-state, meaning that an additional higher magnitude voltage pulse (from the DC power supply) was also passing through the active filter and causing its output response to be greater in magnitude [29]. It was subsequently determined that after shifting the BPM raw input pulse into a steady-state mode of circuit operation, the amplification portion of a single-stage active filter would not produce enough gain to magnify the BPM input signal to a satisfactory level of peak amplitude for downstream components to process. Therefore, two additional stages of amplification and filtering were cascaded together so as to create enough gain for the input signal.
to have its peak amplitude increased sufficiently enough at the output of the final cascaded third stage [29].

The LC bandpass filter of the BPM active filter acts like a tuned resonator in that it is only responsive at the resonant frequency to any amplified sinusoidal currents coming into it. As can be seen in Figure 12, the filter produces an output that is scaled to the input of the active filter at the same resonate frequency. Since the resonator has highest impedance at the resonant frequency, the gain of the active filter is highest at this frequency as well [30].

![Figure 12: Tuned Class C amplifier [31].](image-url)
As seen in Figure 13, the voltage gain for a single stage of the active filter is proportional to the collector current resistance in parallel with the load resistance of the output voltage. In the situation of the BPM active filter, the collector current resistance in the diagram represents the resistance of the LC filter at a specific frequency due to the fact the LC filter’s resistance is frequency dependent. Since the BPM active filter is cascaded into three separate stages, the voltage gain of Stage 1 of the active filter is affected by the loading effects of Stages 2 and 3 on it when computing its load resistance. Likewise, the voltage-gain of Stage 2 is affected the loading effects of Stage 3 on it when computing its load resistance [30].

As seen in Figure 14, the frequency response of the BJT transistor-biased network indicates the linear region of operation of the transistor as well as where the response becomes nonlinear due to the capacitive effects of the network at lower and higher frequencies, as designated by the low and high cutoff frequencies included in the diagram. For lower frequencies, the capacitive effects come from bypass and decoupling capacitors $C_s$, $C_c$ and $C_E$ of the BJT common-emitter circuit network. For higher frequencies, the capacitive effects come from the parasitic capacitances between the collector-to-base and base-to-emitter junctions of the BJT transistor and the parasitic capacitances between the physical external leads of the transistor itself. As can be seen in the same figure, the parasitic effects of the transistor’s performance become apparent at frequencies above the high cutoff frequency point designated in the diagram. The gain of the transistor itself begins to decrease at this frequency, thus causing the transistor to no longer amplify any signal incoming to it. The Miller effect (see Figure 15) occurs from the parasitic capacitance between the collector and base junction of the transistor and can potentially cause the amplification process of transistors in common emitter configuration to become short circuited [28, 32].
a) Voltage gain characteristics (single stage).

\[ \frac{V_o}{V_s} = A_{V, \text{load}} = \frac{-R_L || R_C}{r_e} \]

\[ Z_i = R_C || R_L || \beta r_e \]

\[ Z_o = R_C \]

b) Voltage gain characteristics (cascaded stages.)

\[ A_{\text{total}} = A_1 A_2 A_3 \]

Figure 13: Voltage gain characteristics of BPM three-stage active filter [30].
The AC high-frequency model of a single stage of the BPM active filter is displayed in Figure 16, where the collector current resistor represents the resistance of the LC filter at a single frequency [32]. As can be seen in the figure, the parasitic effects of the active filter at high
frequencies are denoted with dotted lines. The parasitic capacitances are from the leads of the transistor pins and the emitter, collector and base junction regions of the transistor itself. As stated above, the gain of the transistor is adversely affected by the parasitic effects of the transistor and high frequencies and can cause the incoming signal to be attenuated according to the frequency response plot in Figure 14. A transistor parameter of interest is its transition frequency, which is the frequency incoming to the transition at which it produces an output gain of unity [32]. Above the transition frequency, the transistor starts to attenuate the magnitude of input signal components that have a greater frequency than it.

Figure 16: High-frequency parasitic model of BPM active filter [32].
Section 3.4: BPM Timing Trigger Circuit

For the BPM prototype system, the timing trigger circuit will coordinate signaling operations to the sample-and-hold and analog-to-digital chips so that digitization of the elongated and amplified BPM analog signal can successfully occur. The timing trigger circuit is contained on the BPM signal processing board and essentially consists of a summing amplifier, non-inverting amplifier, high speed comparator chip and monostable multivibrator chips that serve as trigger timing devices [33],[34].

The high-speed comparator chip detects the initial amplitude onset of the incoming BPM signal from the signal detector board and then activates the monostable multivibrator chips to generate a trigger signal to the sample-and-hold and analog-to-digital chips, based on the delay times that are configured into the separate monostable multivibrator chips. As illustrated in Figure 17, the output of the first set of cascaded multivibrator chips goes to the “sample/hold” pin on the BPM signal processing sample-and-hold chip and initiates a “hold” operation to occur on that device. The output of the second set of cascaded multivibrator chips goes to the “conversion start” pin on the BPM signal processing analog-to-digital converter chip and initiates an analog-to-digital operation to occur on that device [33],[34].
The timing of the BPM timing trigger circuit is controlled by the monostable multivibrator units that are contained within it. A monostable multivibrator can also be viewed conceptually as an edge-triggered timing circuit that produces a square pulse of fixed duration upon a falling-edge or rising-edge input condition. For the BPM timing trigger circuit, there are a total of four monostable multivibrator chips. Two of them are serially connected to toggle the “sample-and-hold” pin on the BPM signal processing sample-and-hold chip, and two are serially connected to toggle the “start-conversion” pin on the BPM signal processing analog-to-digital converter chip. The first monostable multivibrator chip is triggered by a rising edge from the output of the voltage comparator chip after it detects that an initial voltage onset has occurred for a new elongated and amplified BPM incoming signal [33],[34].
The time duration of the output pulse of the monostable multivibrator chip is controlled by an external capacitor and resistor that are connected to the chip. The resistance and capacitance values can be configured to produce a specific output pulse duration once the pulse is generated via an edge-triggered event from its input signal. For the BPM prototype system, a variable resistor will be used to calibrate the resistance value that corresponds to the proper amount of time that the monostable multivibrator output pulse is to remain in an “on” state [34],[35].

The delay times of the monostable multivibrator chips will be calibrated by connecting an external oscilloscope to the output of the BPM signal detector board and then measuring the amount of time it takes for the elongated and amplified BPM signal to reach its peak value from the reference point of its point of initial (amplitude) ascent. For the measurement to occur, the calibration will be done using the actual BPM input signal as generated by the AWA linear accelerator while in full operation. Since the envelope “rise time” of the BPM signal at the final output of the active filter is always the same, irrespective of its peak amplitude, the calibrated delay time can be “hard coded” into the monostable multivibrator chip via the capacitance and resistance of the external variable resistor and timing capacitor that are on the chip [35].

The datasheet for the monostable multivibrator chip contained on the BPM signal processing board provides a graph that indicates the various capacitance and resistance values that correspond to a given delay time of the output pulse before it transitions from an “on” to “off” state. There are separate graphs for 1.8V, 3.3V and 5V power supplies used to power the chip. The use of the graphs aid in not having to manually compute a specific RC time constant for the external variable resistor and time capacitor pair that corresponds to the desired time delay for the output pulse of the monostable multivibrator chip [35].
As seen in Figure 18, the comparator circuit selected for the BPM timing trigger circuit was the AD8611 chip by Analog Devices. Based on the demands of the BPM timing trigger circuit, the most significant specification parameter of the AD8611 chip is its propagation delay. The propagation delay is the amount of time it takes for the output signal of the comparator to make a 50% transition from a “low” to “high” output level (or vice versa) after the value of the signal at the comparator’s non-inverting input terminal has exceeded the value of the signal at the comparator’s inverting input terminal (or vice versa). Other factors such as temperature, source resistance, overdrive, supply voltage, load capacitance and common mode voltage can also affect the value of the propagation delay on the AD8611 chip. The nominal propagation delay, as it relates to the DC supply voltage of the BPM timing trigger circuit, is listed on the AD8611 datasheet as 4 nanoseconds [33],[36],[37].

Figure 18: AD8611 chip of the BPM timing trigger circuit [34].

The significance of the propagation delay, as it relates to the BPM timing trigger circuit, is that any value associated with it must be factored into the total delay time that is needed between the time an initial onset value of the BPM elongated signal is detected and the time when the
timing trigger circuit signals to the sample-and-hold chip to latch the BPM analog signal that it is continuously tracking. The total delay time that the BPM timing trigger circuit produces should correspond to the time it takes for the filtered BPM analog signal to reach its peak amplitude from the time it begins its initial amplitude ascent. As mentioned previously, the “rise-time” of the filtered BPM analog signal will be determined beforehand using an oscilloscope that is attached to the final output of the active filter that is on the BPM signal detector board. Once this signal waveform is captured and the rise-time of it is measured by the oscilloscope, then calibration of the BPM timing trigger circuit can occur via adjustment of the variable resistors that are on the monostable multivibrator chips contained within it. Therefore, it is the propagation delay of the AD8611 comparator chip in combination with the delay time of the calibrated monostable multivibrator chips that must equal the rise time of the filtered BPM signal (as measured beforehand by an oscilloscope attached to the BPM signal detector board) so that the signaling operation to the sample-and-hold chip to latch the peak amplitude of the BPM signal can successfully and precisely occur. Once fabrication and assembly of the BPM signal processing board is complete, the propagation delay of the AD8611 comparator chip can then be precisely computed [33],[36].

With respect to the AD8611 comparator circuit of the BPM timing trigger circuit, the reference signal (into the inverting input terminal) and the input signal (into the non-inverting input terminal) have common mode and differential components. The common mode component (which is the average value of both signals) is implemented using a parallel voltage divider from the on-board DC power supply so that the reference voltage and input voltage are at a nominal 2.5 volts. For the reference voltage, a shunt bypass capacitor is used to redirect any AC components
contained in the signal to ground, so that the reference voltage of the comparator input remains fixed at 2.5 volts. The common mode voltage range, as specified in the AD8611 datasheet, is between 0 and 3 volts [33],[38].

As seen in Figure 19, the input signal into the AD8611 chip is the elongated BPM signal from the signal detector board after it has passed through both summing and inverting amplifiers on the BPM signal processing board. A decoupling capacitor is also located between the inverting amplifier and AD8611 chip so as to block the DC component of the elongated BPM signal from entering into the non-inverting input of the AD8611 chip. As seen in Table 1, the datasheet specification for the input voltage range of the AD8611 chip (having a positive and negative DC power supply voltage of Vcc and Vee respectively) is from \( Vcc + 0.3V \) to \( Vee - 0.3V \). The AC-filtered portion of the BPM signal then acts as the differential portion of the non-inverting terminal of the AD8611 chip, with the common mode portion of it being 2.5 volts from the voltage divider circuit that it is interconnected with at the point of entry into the non-inverting terminal of the AD8611 chip.
Figure 19: Summing amplifier, inverting amplifier and AD8611 chip of the BPM timing trigger circuit [34].

Table 1: Attributes of BPM AD8611 Comparator Microchip [33]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Propagation delay</strong></td>
<td>4ns</td>
</tr>
<tr>
<td><strong>Common mode input voltage</strong></td>
<td>0V to 3V</td>
</tr>
<tr>
<td><strong>Differential mode input voltage</strong></td>
<td>-5V to +5V</td>
</tr>
<tr>
<td><strong>Input voltage range</strong></td>
<td>$V_{ee} - 0.3V$ to $V_{cc} +0.3V$</td>
</tr>
<tr>
<td><strong>Offset voltage (maximum)</strong></td>
<td>7mV</td>
</tr>
<tr>
<td><strong>Maximum input frequency</strong></td>
<td>100MHz</td>
</tr>
</tbody>
</table>

As seen in Figure 20, the summing amplifier of the BPM timing trigger circuit is used to sum the incoming filtered analog signals from each of the four BPM signal detector boards (right, left, top and bottom with respect to which BPM button pickup they are attached to) via an external DB-15 ribbon connector that is on the BPM signal processing board. The frequency bandwidth of
the summing amplifier matches that of the AD783 sample-and-hold chip so that it can act on all of the frequency components inherent in the BPM analog signal as filtered by the BPM signal detector board. After summing the incoming inputs, two clamping diodes are used to limit the output voltage so as to keep it in the proper voltage range after the summing operation of the summing amplifier has occurred [33],[38].

Figure 20: BPM signal processing board DB-15 ribbon connector and summing amplifier of the BPM timing trigger circuit [34].

The summed BPM signal is then fed into an additional amplifier that amplifies it further so that it can more rapidly exceed the offset voltage of the AD8611 comparator chip once a zero-crossing condition of the BPM signal has occurred. The offset voltage for the AD8611 chip is a maximum of 7 millivolts. After the BPM signal is further amplified for this purpose, a decoupling capacitor at the output of the amplifier removes the DC component of the signal so that it may stay within the positive input voltage range of the AD8611 comparator chip, which is $Vcc+0.3$ volts. For the BPM signal processing board, the DC power supply voltage $Vcc$ is 5 volts [33],[34].
Section 3.5: Sample-and-Hold Circuit

For the BPM prototype system, the AD783 chip by Analog Devices is the chip that is used to track and latch an individual BPM input signal after it has been elongated and amplified on the BPM signal detector board. There are a total of four separate AD783 chips on the BPM signal processing board, one for each of the different BPM signal detector boards that comprise the entire BPM prototype system. The analog input into the AD783 chip is the BPM elongated signal from the corresponding signal detector board it is connected to via a DB-15 female connector mounted onto the signal processing board. The AD783 chips are powered by a 5V DC power supply that is housed on the signal processing board as well. The output of each AD783 chip is connected directly to a different channel input on the ADC chip that is responsible for digitizing the “latched” BPM analog signal.

For the purposes of the BPM prototype active filter on the signal detector board, the sample-and-hold circuit is used to latch the elongated and amplified BPM input signal so that it can be properly digitized afterward by the analog-to-digital converter chip on the BPM signal processing board. The sample-and-hold attributes of greatest importance (from the perspective of BPM active filter) are the small-signal bandwidth and the aperture delay time. As displayed in Table 2, the AD783 sample-and-hold circuit has a small-signal bandwidth of 15MHz. This means that all frequency components of the elongated BPM incoming signal must lie within this bandwidth for the sample-and-hold operation to correctly sample (i.e., track) and hold the amplitude of it for any duration of time. This is the primary reason why a bandpass filter is used within the active filter of the BPM signal detector board, so that all frequency components of the
resulting filtered BPM signal lie within the frequency bandwidth of the AD783 sample-and-hold chip [39],[40].

Table 2: Attributes of BPM AD783 Sample-and-Hold Microchip [39]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small-signal bandwidth</td>
<td>15MHz</td>
</tr>
<tr>
<td>Aperture delay time</td>
<td>15ns</td>
</tr>
<tr>
<td>Full-power bandwidth</td>
<td>2MHz</td>
</tr>
<tr>
<td>Droop rate</td>
<td>0.02 uV/us</td>
</tr>
<tr>
<td>Hold mode settling time</td>
<td>150ns</td>
</tr>
</tbody>
</table>

The other sample-and-hold circuit attribute of greatest significance (from the perspective of the BPM signal detector board) is the *aperture delay time*, which is the amount of time that elapses between when the “hold” pin on the AD783 chip is pulled “low” and the “sampling” switch on the chip fully disconnects from the charging capacitor that tracks the analog input signal coming into the sample-and-hold circuit. The typical aperture delay time for the AD783 chip is 15ns. During this time of delay, any changes in amplitude of the analog input signal being tracked can contribute to jitter error, which is based on the rate at which the analog input signal changes over time. Therefore, the BPM raw input signal must be elongated such that the amplitude of the peak region of the signal fits within the 15ns aperture delay window of the AD783 chip. In other words,
the rate of change of the elongated BPM signal must be minimized so that any significant variation in amplitude of the signal does not occur while the aperture delay time is in effect once a “hold” operation on the AD783 chip has been initiated [39],[40].

To a lesser extent, another attribute of importance, from the perspective of the BPM active filter on the signal detector board is the full-power bandwidth of the sample-and-hold circuit. For the AD783 chip, the full-power bandwidth is 2MHz. This is the frequency at which the amplitude of an incoming signal component coming into the sample-and-hold circuit, and equal in magnitude to the maximum voltage allowed, is attenuated by an amount greater than 3dB. For the AD783 chip, the maximum incoming voltage allowed is 5 volts [39],[40].

From the perspective of the BPM timing trigger circuit, the SAH circuit attributes of greatest importance are its droop rate and hold mode settling time. The droop rate is the rate at which the SAH circuit’s “tracking” capacitor leaks current while in hold mode. For the AD783 chip, the droop rate is 0.02 \( \mu \text{V/\mu s} \). Due to the tracking capacitor’s leakage of current while in hold mode, the droop rate of the sample-and-hold circuit must be taken into account when determining an upper bound for when the ADC conversion of the latched signal should begin. The other SAH parameter of interest, the hold mode settling time, is the amount of time it takes for its output voltage to reach a steady-state value after a hold operation is initiated on the analog signal that it is tracking. For the AD783 chip, the hold mode settling time is 150ns. Therefore, the BPM timing trigger circuit must be configured such that it does not initiate a “conversion start” signal to the interconnected ADC chip until at least 150ns after it has initiated the sample-to-hold operation on the AD783 chip. Furthermore, it must also initiate the same “conversion start” signal to the ADC
chip before exceeding the time constraints of the droop rate, wherein an appreciable amount of voltage across the tracking capacitor is lost. [39],[40].

Section 3.6: Analog-to-Digital Converter Circuit

For the purposes of the BPM prototype system, digitization of the elongated and amplified input raw signal is accomplished by the analog-to-digital converter (ADC) chip that is on the BPM signal processing board. The ADC converter selected for this task is the AD7091R-8 ADC chip by Analog Devices Corporation (see Table 3). As seen in Figure 21, it converts the peak value of the elongated and amplified BPM signal received from the adjacently connected sample-and-hold AD783 chip and provides the digitized result to an externally connected hardware module via a serial peripheral interface (SPI) bus that is connected between it and the AD7091R-8 chip [38].

Table 3: Attributes of BPM AD7091R-8 ADC Chip [38].

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-power bandwidth</td>
<td>1.5MHz</td>
</tr>
<tr>
<td>Aperture jitter</td>
<td>40ps</td>
</tr>
<tr>
<td>Throughput rate</td>
<td>1 MSPS</td>
</tr>
<tr>
<td>Total harmonic distortion</td>
<td>-80dB</td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>70dB</td>
</tr>
<tr>
<td>Number of bits</td>
<td>14</td>
</tr>
<tr>
<td>ADC conversion time</td>
<td>600ns</td>
</tr>
</tbody>
</table>
Figure 21: SAH and ADC interface (BPM signal processing board) [34].
An ADC conversion request is initiated by the synchronization unit of the BPM signal processing board that detects the presence of the peak value of the BPM elongated input signal and then pulls low the “initiate ADC conversion” pin on the AD7091-8 chip so as to initiate digitization of the analog BPM signals that it samples from the outputs of the AD783 SAH chips that are hardwired into it. The AD7091R-8 chip has been configured (via internal hardware registers) to have one of its external pins used as BUSY indicator to an external device that receives digitized data from it via its external SPI bus. For the BPM prototype design, and as seen in Figure 22, a Raspberry-Pi chip was selected to interface with the AD71091R-8 chip via the SPI bus such that it acts as the “master” device and the AD71091R acts as the “slave” device [34]. In this configuration, the BUSY pin of the AD7109IR chip is hard wired to one of the general-purpose IO pins on the Raspberry-Pi single-board computer (Table 4) so that it can trigger an edge-triggered interrupt after a digitization sequence has completed, which is signified by the BUSY pin on the AD71091R chip going from low to high (or vice versa). The edge-triggered interrupt can then invoke a custom-written interrupt service routine on the Raspberry-Pi that initiates the retrieval of digitized BPM data from the ADC chip via the SPI interface that functions as the data bus between the AD7109R chip and Raspberry-Pi single board computer[38].
Figure 22: ADC and Raspberry-Pi interface (BPM signal processing board) [34].

Table 4: Attributes of Raspberry-Pi Single-Board Computer [41]

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM-based system-on-a-chip (SOC) processor</td>
<td>Pulse-width modulation (PWM interface)</td>
</tr>
<tr>
<td>DMA controller interface</td>
<td>Serial peripheral interface (SPI)</td>
</tr>
<tr>
<td>UART serial interface</td>
<td>Broadcom serial controller (BSC) interface</td>
</tr>
<tr>
<td>Programmable external/internal timer interrupts</td>
<td>Pulse-code modulation (PCM) audio interface</td>
</tr>
<tr>
<td>General-purpose input/output (GPIO) interface</td>
<td>Inter-integrated circuit (I2C) serial interface</td>
</tr>
</tbody>
</table>
A single ADC operation on the AD7091R-8 chip takes 600ns to complete. The conversion action itself is initiated when the “conversion start” external pin of the AD7091R-8 is pulled low by the external device that is facilitating the synchronization of ADC operations to occur. In the case of the BPM prototype signal processing board, this is done by the timing trigger circuitry on the BPM signal processing board when it detects an elongated BPM signal from the output of the BPM signal detector board. Once the initiation of a “conversion start” operation occurs, the AD091R-8 signifies that a ADC conversion is in progress by pulling its BUSY external pin either low or high, depending on how it has been configured by the “master” device of the SPI interface. The Raspberry-Pi controller, which is the “master” device of the SPI bus connected to the AD091R-8, will then acquire control of the SPI bus (by pulling the SPI bus “chip select” pin low) and issue an SPI “read ADC data” command to the AD091R-8 chip [38].

In order to digitize the multiple analog BPM inputs that are fed into the AD091R-8 from the output pins of the SAH chips that are connected to it, a separate “conversion start” action must be initiated from the external device that is driving its operation. The AD901R-8 chip has a separate configurable SPI register, each bit of which corresponds to a separate ADC channel that is connected to the analog signal that it is externally hardwired to. The minimum time required between separate analog-to-digital conversions on the AD091R-8 chip is 1 microsecond. For the system requirements of the BPM prototype system, this does not pose a problem because the repetition rate of incoming raw BPM signals into the BPM signal detector board is only about 5 Hz [38].
Section 3.7: Raspberry-Pi Computer Interface

For the purposes of the BPM prototype system, the Raspberry-Pi board that is accessed via a single 40-pin general-purpose input-output (GPIO) connector that is connected to the BPM signal processing board (see Figure 23) acts as the repository of digitized BPM raw input data after it has been amplified and elongated via the multi-stage active filter on the BPM signal detector board and converted from analog-to-digital form via the sample-and hold and analog-to-digital chip components that reside on the BPM signal processing board. The Raspberry-Pi board retrieves the digitized BPM data from the analog-to-digital chip on the signal-processing board via a serial peripheral interface (SPI) bus that connects both devices together. In this capacity, the Raspberry-Pi board acts as the SPI “master” device and initiates the transfer of digitized BPM data to it whenever it receives notification from the ADC chip that a new analog-to-digital conversion of data has taken place [38, 41].

Figure 23: Raspberry-Pi GPIO connector [42].
The manner in which digitized BPM data from the ADC chip is transferred to the Raspberry-Pi board is by the latter monitoring the “conversion busy” pin on the ADC chip. The logic level of this pin is pulled “high” by the ADC chip whenever an ADC conversion operation begins and is pulled “low” by the ADC chip whenever the ADC conversion operation ends. On the printed circuit board of the BPM signal processing board, the ‘busy’ pin from the ADC chip enters directly into one of the GPIO pins of the Raspberry-Pi board. Therefore, this GPIO pin on the Raspberry-Pi board can be monitored to determine when it should read newly digitized BPM data from the ADC chip. The facilitation of this task can be most effectively accomplished by assigning a falling-edge interrupt to the aforementioned GPIO pin so that once a falling-edge condition is detected on it, an interrupt condition occurs that then permits the Raspberry-Pi board (via a custom-written interrupt service routine) to initiate the appropriate transfer-of-data commands from it to the ADC chip via the SPI bus so as to retrieve the newly digitized BPM data from it in an asynchronous manner [38],[41].

Since the AD7091R-8 ADC chip is designed as a SPI “slave” device, the Raspberry-Pi board, as SPI “master” device, is responsible for initiating all data transfers via the SPI bus between itself and the AD7091R-8 chip. This is accomplished by the use of several SPI hardware registers on the ARM-based System-on-a-chip (SOC) integrated circuit that is on the Raspberry-Pi board. With respect to the SPI interface, the two most important hardware registers are the SPI_Master_Control_and_Status and SPI_Master.Tx_and_Rx_FIFO registers. The former is responsible for indicating when a SPI data transfer is in progress, generating an interrupt once a SPI data transfer operation is complete or indicating when a SPI internal input/output buffer is full. The latter functions as a buffer register that initiates and sustains the SPI clock bus cycles and
physically transfers all data written to it over the SPI bus. In a majority of cases, access to hardware registers on a SoC circuit are typically done via system calls from multi-threaded application programs to the hardware device drivers of the operating system that run on the Raspberry-Pi board.

Another purpose that the BPM Raspberry-Pi computer serves is to activate various attenuation relays that are connected between the signal detector board and corresponding BPM button pickup that it is connected to. Once proper attenuation of the signal (within an acceptable predetermined range) takes place, then processing of the attenuated signal (by the signal detector board) can occur. This is facilitated in the BPM signal processing board design by allocating five separate general-purpose input-output (GPIO) pins (that are on the Raspberry-Pi board) to each of the separate external attenuation relays. Each of these GPIO outputs is then fed into an external transistor array chip on the BPM signal processing board that boosts the voltage level of the GPIO signal to a level that can then drive the attenuation relays on the signal detector board when attenuation of the BPM raw incoming signal needs to occur. After the voltage level of the attenuation relay signal has been boosted, it is then routed to the external relays via an external DB-25 ribbon connector that is mounted to the BPM signal processing board. Each one of the aforementioned GPIO pins corresponds to a different charge magnitude of various beam bunch particles that can be accelerated by the particle accelerator [41],[43].

The BPM attenuation relay outputs on the Raspberry-Pi board are enabled or disabled by a human operator working from a remote host computer that is connected to the Raspberry-Pi computer via an external ethernet connection. Once the human operator determines the charge level of the particle beam that is to be accelerated, he can input this value into a custom-written
application program that runs on the host computer. This application program can then send the charge level information (via TCP-IP socket connection) to an application client program that is running on the BPM Raspberry-Pi board. Upon receiving and decoding the charge level information, the client program can then, via the appropriate GPIO hardware register, enable and/or disable the corresponding on-board relay-assigned GPIO pins that are connected to the external attenuation relays via the DB-25 ribbon connector that is mounted to the BPM signal processing board [41],[43].
In its original form, signal conditioning on the BPM prototype system was accomplished using a standard peak rectifier circuit consisting of a diode, capacitor and resistor. As seen in Figure 24, the raw incoming signal from the BPM button pickup was fed into the peak rectifier circuit, and during the positive half-cycle, the capacitor tracked the voltage of the incoming signal while the diode remained in forward-biasing mode. After reaching the peak of the incoming signal, the diode would become reverse-biased and no longer conduct, thus causing the capacitor to effectively latch the peak signal and then slowly discharge through the resistor at a rate determined by the RC time constant of the circuit. Due to the slow discharge-rate of the capacitor, the incoming BPM signal could therefore be stretched out in time [25].
Using this initial circuit topology, the width of the raw incoming BPM signal was effectively elongated from 100 picoseconds to 30 nanoseconds. Further elongation of the signal was achieved by reconfiguring the circuit to activate, via relay switches and jumper pins, capacitors of different capacitance based on the charge level inherent in the BPM-induced signal. This functionality caused elongation of the BPM signal to go from 30 nanoseconds to 300 microseconds for a 30 nano-coulomb bunch charge. Using the capacitor switching network for different voltage levels of the incoming BPM signal, beam charge levels down to 100pC could be successfully detected and elongated in time [25].

An initial setback in the functionality of the peak rectifier circuit as described above was related to its inability to correctly process BPM signals that were induced from low-charge accelerated particle beams. Specifically, there is a voltage threshold level below which the diode will not conduct. In scenarios such as this, the peak rectifier circuit becomes inactive due to the lack of any current flowing through it. Typically, the threshold voltage level for diodes to conduct current is approximately 700 millivolts. So in the case of the initial BPM signal conditioning circuit, this constraint posed a sensitivity issue for detecting BPM incoming signals induced from a beam bunch having a charge level in the pico-coulomb range [25].
Experiments were then carried out by connecting the BPM incoming raw signal to a standard RLC circuit to see if such a configuration would in any way improve sensitivity to the input range of the BPM signal. The idea behind this configuration was to try and avoid the voltage threshold constraints of the diode-based peak-rectifier design and use a resonator circuit instead to process and elongate the BPM raw signal. Further testing revealed that the lower bound sensitivity to the raw BPM signal using this configuration was to a beam charge level of 2 nano-coulombs. So it was confirmed again that pertaining to input-signal sensitivity, both initial signal conditioning circuit configurations were unable to successfully detect incoming BPM signals within a 1pC to 2nC range [25].

Afterward, the BPM prototype system consisted of a basic peak detector circuit, differentiator circuit, comparator circuit and analog-to-digital converter chip. The raw incoming BPM signal (from the BPM electrode) would first be fed directly into the input of the peak detector circuit. After capturing the peak amplitude of the signal, the peak detector output would then be fed into a differentiator circuit. The differentiator circuit was a standard configuration of a differentiator operational amplifier. The purpose of the differentiator circuit was to detect the peak value of the signal via an instantaneous slope value of (or near) zero. A comparator circuit connected to the output of the differentiator circuit and configured to trigger when detecting an input voltage condition of zero volts would then trigger and cause the ADC chip to initiate a new ADC conversion at each of its analog inputs [44].

A preliminary single-stage active filter was then designed to amplify and then filter the incoming BPM raw signal such that it could be elongated by removing the higher frequency components of the signal. As displayed in Figure 25, the active filter consisted of a standard bipolar
junction transistor (BJT) circuit in common emitter configuration to amplify the BPM signal and
an LC bandpass (i.e., damped resonator) filter connected to the collector pin of the transistor so as
to give a damped output response at its resonant frequency. As seen in the same figure, initial
simulation results revealed that the active filter had an input sensitivity range between 0.05 volts
to 8.0 volts, which corresponded to 17pC and 2.67nC beam charge levels (where using anecdotal
methods of measurement, 1pC of charge approximately maps to 3mV of electrode button voltage
[26]) and, in its under-damped filter response, elongated the pulse width of the incoming BPM
signal to approximately 380 nanoseconds [25].

![Figure 25: Schematic and simulation results of BPM single-stage active filter using
BJT transistor in common emitter configuration [25].](image)

The idea behind using the LC filter was for it to act as a resonator for a small range of
frequencies such that the output response for the bandpassed components would be minimally
damped and strong in magnitude. It was important to have a center frequency of the LC filter such that most of the high frequencies of the incoming BPM signal, which are principally in the RF L-band (i.e., 1 GHz to 2 GHz) range, would be attenuated such that the damped-output response signal is no longer RF in nature and has frequency components that are bandwidth compatible with the sample-and-hold and comparator circuits on the BPM signal processing board. It is also critical for the filtered BPM signal to be depleted of high-frequency content in RF range so that the parasitic effects of the signal are greatly lessened on other downstream lumped components that are on the signal detector and signal processing BPM boards [25].

It was later discovered in additional testing that the output signal of the initial active filter had a transient signal response superimposed upon it that gave misleading information regarding its envelope shape and peak magnitude. To be specific, the simulation of the incoming raw BPM signal was done beginning at time zero, which corresponds to a powering-up condition of the circuit. Because of the power supply switching operation at power-up of the circuit, a transient signal from the switching operation passed through the active filter concurrently with the BPM raw input signal. The output response of the active filter was therefore the superposition of both signals passing though it at the same time [25].

The active filter was also later tested with simulated BPM raw signals that were scaled to a much finer scale of resolution. During the initial testing of the active filter, the raw BPM signal had a scaling factor of between 1 and 20, but similar simulation testing at a later time used a scaling factors of 0, 0.5, and 1 and revealed a negligible magnitude response at the output of the active filter. The scaling factor of the raw input signal is a way to mimic different particle beam charge levels that can induce the BPM signal. The weak response of the single-stage active filter indicated
that it would not be able to sufficiently amplify the incoming BPM signal to the point where it could be successfully detected by downstream components on the signal processing board [25].

As seen in Figure 26, the initial design of the BPM signal processing board consisted primarily of five different sub system components: BPM signal buffers, analog-to-digital converter, DSP controller interface, differentiator circuit, and comparator circuit. Initially, the BPM signal processing board was intended to receive BPM signals from eight different peak detector boards that correspond to two separate BPM units. Since each BPM interface contained four different signal detector boards (one for each electrode embedded within the beam-pipe walls of the particle accelerator itself), there were a total of two different BPM interfaces that the signal processing board would be able to interact with. The various BPM signals that had undergone signal conditioning on the signal detector boards were fed into the BPM signal processing board via a DB-15 connector that was attached to it [25].
The differentiator circuit on the BPM signal processing board was designed to detect the peak value of the BPM signal from the peak detector that performed signal conditioning on the raw incoming BPM signal. Since the output of the differentiator circuit is essentially the instantaneous slope of the BPM signal, its peak value could be signified by an output value of the differentiator circuit that was approximately zero. The output of the differentiator circuit could then be used as a triggering mechanism to determine when a given ADC operation should occur once the BPM peak value is detected via the operation of the differentiator circuit. The LM318
operational amplifier by Texas Instruments was chosen as the op-amp for the differentiator circuit [25, 45].

The analog-to-digital converter selected for the initial BPM signal processing board was the LTC2358-18 ADC chip by Analog Devices. As seen in Table 5, it supported 16-bit data conversion and had eight separate analog input channels from which digitization could simultaneously occur. The LTC2358-18 chip was to be powered by the 12-volt DC power supply on the BPM signal processing board. The ADC operation on the LTC2358-18 chip is initiated by pulling low the “conversion start” pin on the chip which the comparator (at its output) does when the peak value of the incoming BPM signal is detected by the differentiator circuit to which it is connected [25, 46].

Table 5: Attributes of BPM LTC2358-18 ADC Microchip [46]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3dB bandwidth</td>
<td>6 MHz</td>
</tr>
<tr>
<td>Aperture jitter</td>
<td>3 ps</td>
</tr>
<tr>
<td>Throughput rate</td>
<td>200ksps</td>
</tr>
<tr>
<td>Total harmonic distortion</td>
<td>-111dB</td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>94.2dB</td>
</tr>
<tr>
<td>Number of bits</td>
<td>16</td>
</tr>
<tr>
<td>ADC conversion time</td>
<td>500ns</td>
</tr>
</tbody>
</table>
From its initial design, the DSP controller for the BPM signal processing board was a Raspberry-Pi-based computer. The primary function of the Raspberry-Pi board is to intercept digitized data from the LTC2358-18 ADC chip via a SPI interface between the two devices. The Raspberry-Pi board also was needed to activate various relays that were on the front end of the BPM signal detector board so as to attenuate the voltage of incoming raw BPM signals and/or activate appropriate tracking capacitors on the peak detector circuit so that its output voltage could maintain a desired voltage level based on the ratio of the beam charge level of the incoming BPM signal and the capacitance of the capacitor selected via the appropriate relay that corresponds to it [25].

Buffer amplifiers were also placed between the BPM signal inputs from the DB-15 connector on the signal processing board and the LTC2358-18 ADC chip that digitized the filtered BPM analog signal from the signal detector board. The buffer amplifiers were utilized to prevent unwanted loading between the BPM signal detector board and the LTC2358-18 ADC chip on the signal processing board. The buffer amplifiers chosen were LM318N operational amplifiers by Texas Instruments and, in accordance with the datasheet guidelines, were configured in a voltage follower topology [45].

The original design of the BPM signal processing board also contained a digital-to-analog converter on it. The DAC component was intended to be part of a closed-loop feedback system where beam tuning could occur based on the beam position information extrapolated from the digitized peak amplitudes of BPM elongated signals coming from the four BPM signal detector boards. It was afterward decided that any such processing, if needed, could be done on a separate
computer that received the digitized peak amplitude of the BPM signals via a peripheral interface with the Raspberry-Pi DSP controller on the BPM signal processing board [25].

Several problems with the circuit components (as described above) were discovered that rendered the design as inviable for future use. In particular, through simulation testing it was discovered that the diode of the peak detector on the BPM signal detector board had a reverse-biased parasitic capacitance that permitted higher frequency components of the incoming BPM signal to pass through it and adversely affect the detector’s ability to correctly latch the peak BPM raw incoming voltage. Moreover, through additional testing it was determined that the diode was not acting in a linear fashion for incoming BPM signals that were in the few-millivolt range. As a fundamental constraint on the design of the BPM signal detector board, it is required that its input and output voltages have a linear response over the entire range of input signals that can be generated from the BPM electrode pickups [44].

An additional problem that was later discovered was that the differentiator circuit on the BPM signal processing board had a propagation delay time that prevented it from creating a low-latency signaling condition once it detected the peak magnitude of the elongated BPM signal. In a scenario such as this, the output of the differentiator would be approximately zero (corresponding to a slope of zero for the peak magnitude of the BPM signal) and act as the threshold value for the comparator circuit that it was attached to. Because of the propagation delay, though, the amount of time for the comparator circuit to initiate a trigger signal to the ADC chip (via its “conversion start” pin) would be delayed and cause the ADC chip to digitize the BPM signal at the wrong time [47].
To remedy this problem, additional programmable timing circuits were utilized on the BPM signal processing board to replace the differentiator circuit and delay the triggering mechanism of the comparator circuit by a pre-calibrated amount of time. As seen in Table 6, the timing circuit chosen was the SN74LVC1G123 monostable multivibrator chip by Texas Instruments. The delay time of the chip was configured using a capacitor and potentiometer and was designed to be externally connected to it. This would then require that the rise time of the elongated BPM signal be measured using an oscilloscope connected to the output of the active filter on the BPM signal detector board [35, 47].

Table 6: Attributes of SN74LVC1G123 Monostable Multivibrator chip [35]

<table>
<thead>
<tr>
<th>DC supply voltage (Vcc)</th>
<th>1.65 to 5.5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. high-level input voltage</td>
<td>0.7 *Vcc</td>
</tr>
<tr>
<td>Max. low-level input voltage</td>
<td>0.3 * Vcc</td>
</tr>
<tr>
<td>Output voltage</td>
<td>0 to Vcc</td>
</tr>
<tr>
<td>High-level output current</td>
<td>-32mA</td>
</tr>
</tbody>
</table>
The BPM prototype system consists of two electronic circuit boards, the first of which is the BPM signal detector board that intercepts a raw pulsed-RF incoming BPM signal from the particle accelerator (via attached button electrode plates) and then conditions it via a three-stage active filter into non-RF form. The conditioned (i.e., elongated and amplified) signal is then digitized on an interconnected BPM signal processing board via signaling operations to the sample-and-hold circuit on it that tracks and holds the incoming elongated BPM signal peak voltage so that its peak amplitude can be precisely latched and then converted from analog to digital form.

The design of the two prototype boards was done at Argonne Wakefield Accelerator (AWA) Facility in Lemont, Illinois, primarily by their in-house electrical engineer and is an adaptation of beam position monitoring system schematic diagrams that were previously designed (but not fully implemented) at their facility. Additional assistance in the implementation of the BPM signal detector board was also provided by appropriate students/staff within the Physics and Electrical Engineering Departments at NIU who worked closely with Argonne to implement, test, and/or oversee the development of said BPM prototype system as part of the Chicagoland Accelerator Science Traineeship (CAST) program and a grant awarded to NIU by the United States Department of Energy.

The hardware design for the BPM prototype system was done using the freeware electronic circuit design software package KiCad, so as to create the lumped component schematic diagrams
for the BPM prototype signal detector and signal processing boards. Once individual circuit lumped components and their physical dimensions (i.e., footprints) were identified and input into the BPM signal detector schematic environment, a printed circuit board (PCB) netlist was then generated automatically by the KiCad design software. The spatial topology of the netlist generated was afterward adjusted manually so as to reflect the degree to which board components were supposed to be physically spaced apart, especially as it related to any adverse parasitic effects that could otherwise occur from improper spacing between adjacent traces and/or reactive components on the BPM signal detector printed circuit board.

The next step in the implementation methodology of the BPM prototype signal detector board was to fabricate it via an automation feature of the KiCad electronic circuit design software. The fabrication process is when the prototype board is physically built and all traces on it (i.e., wire connections between hardware components on the board) are physically embedded within the substrate material that overlies the common ground plane of the BPM signal detector prototype board. Fabrication of the BPM signal-detector prototype board was outsourced to an appropriate third-party company and was then sent back to the Argonne facility after fabrication of the board was complete.

After fabrication of the BPM prototype board occurred, the individual electrical lumped components as included in the corresponding KiCad schematic diagrams were attached to it. The electrical components included in the prototype schematic design were either surface-mount devices or through-hole devices. As seen in Figure 27, for surface-mount device (SMD) components, the printed circuit board contains no drilled-in holes for them but rather a conducting surface upon which the SMD components were to reside (see Figure 28). For through-hole-device
(THD) components, the fabricated printed circuit board contained drilled holes at the place where external pins of a given THD component were to be placed. A SMD component is permanently attached onto the printed circuit board surface by applying a heated solder paste underneath the component (via a solder paste gun) and then heating the board via a reflow-soldering-oven process. The reflow soldering oven has a conveyor belt upon which the printed-circuit-board, containing the solder-pasted SMD components, is placed. As it travels down the conveyor belt, the printed circuit board is heated and cooled at various temperatures and in various stages until such time that the soldering process is permanent and complete.

Figure 27: Printed circuit board (PCB) layout for BPM prototype RFFE board.
Figure 28: SMD soldering stages of BPM prototype RFFE board [48].

For the BPM signal detector prototype board, the only SMD elements on it are the inductor components as contained in the signal detector schematic diagram. All other electrical components on the board are THD components. Traditional soldering methods were used to attach the THD components to the signal detector printed circuit board by placing the pins of each THD electrical component through the holes on the printed circuit board that correspond to it and are based on the physical dimensions (as stated in the datasheet) for each THD component. The soldering of the THD components was done using a traditional soldering iron and solder wire so as to fuse the metal connectors of the THD component and solder wire together onto the back of the printed circuit board. For the BPM prototype board, the soldering process was done at both Argonne Wakefield Accelerator (AWA) laboratory and at the Microelectronics Research and Development Laboratory (MRDL) at Northern Illinois University.
Section 4.3: Testing of BPM Prototype System

Bench testing of the BPM signal detector prototype board consisted of performing preliminary testing on the signal detector board so that the output signals of the same could be measured against various input signal permutations using real-world testing equipment such as oscilloscopes, external power supplies, waveform generators and/or voltage/current probe measuring devices. In this scenario, the device under test (DUT) was the BPM signal detector prototype board that was fabricated and assembled together as described above. As stated above, the purpose of the bench testing experiments was to ascertain how the BPM prototype board responded (in terms of basic functionality) to input signals fed into it that, in terms of their pulse widths, moderately resembled those the actual target system (i.e., linear accelerator) itself.

Bench-testing of the BPM signal-detector board was done independently at Argonne Wakefield Accelerator and at Northern Illinois University (see Figure 29). The bench-testing phase of testing the BPM prototype signal detector board is to reveal any necessity of modifications to it so as to more closely align its functionality to the original design and performance constraints of the signaling and data acquisition hardware components on the BPM signal processing board. Once bench testing was complete, testing of the signal detector prototype board on the target system began. For this form of testing, the target system refers to the actual linear particle accelerator system that resides at the AWA facility.
The installation and testing of the BPM signal detector prototype board on the target system was done by having the AWA particle accelerator accelerate a beam of charges to induce a pulsed-RF input signal into the signal detector board via the interconnected BPM button electrode that is embedded within the beam-pipe walls of the accelerator. The internal environment of the target system will also generate various forms of random noise superimposed onto the raw incoming BPM signal, such that proper filtering and/or attenuation of the noise components by the BPM signal detector board can be observed by examining the final elongated and amplified output signal as seen by the BPM signal processing board. Successful testing of the BPM signal detector board on the target system is what brings final validation to fulfilling its original design requirements as specified by the AWA facility.
One of the main limitations in testing the BPM signal detector prototype board was in generating a BPM input signal with full-width-at-half-maximum (FWHM) pulse width close to that of the FWHM width generated at AWA on the linear accelerator that they have at their facility. The AWA facility houses the target system upon which the BPM signal detector board is intended to run and generates a BPM input-signal FWHM pulse width of approximately 800 picoseconds. The lab equipment housed within the Engineering Building at Northern Illinois University can generate a signal pulse width of between 10 and 20 nanoseconds. Due to the system specifications upon which the BPM signal detector prototype board was designed, an incoming BPM signal with a time duration in the nanosecond or microsecond range may cause the voltage level of the output signal of the signal detector board to lie outside the range for which it was originally designed. In such a scenario as this, malfunction of other hardware components on the BPM signal detector and/or signal processing prototype board may afterwards occur.

In such a scenario, one possible reason why the voltage increase at the final output of the signal detector board occurs has to do with the Fourier transform time scaling property that states that stretching a signal in the time domain corresponds to compressing the signal in the frequency domain. The Fourier time scaling property can be stated as:

\[ f(at) \leftrightarrow \frac{1}{a} F \left( \frac{w}{a} \right) \]

\[ \text{where: } a > 0. \]

When stretching a signal in time, \( a < 1 \) and the magnitudes of the compressed frequency components in the spectrum become larger. For this explanation to be asserted definitively, additional experiments with the stretched-out BPM input signal and the BPM signal detector board
need to be performed and the output results judiciously compared so that confirmation of the same can occur [49].

The manner in which research for this study will be carried out is experimental and quantitative in nature. By experimental is meant that the research questions will be validated (or invalidated) by means of specific experiments carried out on the prototype system, the outcomes of which can be measured and quantified (using high-precision instrumentation and calibration equipment) to within the desired degree of accuracy that the experiments require.

For example, there is a range of input voltage signals that are expected to arrive into the BPM signal-detector board that is in proportion to the range of different kinds of charge-beams that are accelerated in particle accelerator. The charge-magnitude of the beam-bunch can vary from roughly 10 pico-coulombs to 100 nano-coulombs, so a corresponding voltage for each charge level can be expected to occur. A calibration process was previously done at the AWA facility to map various charge levels of beam bunches to their corresponding voltage levels as seen from the BPM button pickup electrodes via coaxial cables and measuring equipment that were connected to them [25].

The BPM signal detector prototype board is expected to act on an incoming raw analog signal that has a pulse width of very short duration, typically in the hundreds of picoseconds range. The pulse width is proportional to the speed at which the beam of charged particles passes above/below the BPM electrode plates that are attached to the BPM signal detector board. Due to the fact the beam of charged particles is being accelerated to speeds close to the speed of light, the voltage that it induces on the BPM electrode (i.e., capacitor) plates is of very short duration, only
on the order of hundreds of picoseconds. This hundreds-of picoseconds width is then the reference point from which the BPM active-filter circuitry (in terms of elongating the signal) is designed.

Since two of the goals in the design of the BPM active filter are to elongate and amplify the incoming voltage signal, a critical dimension in this endeavor is to elongate the raw BPM incoming signal to such an extent that it can be processed by the sample-and-hold circuit on the BPM signal processing board. The choice of sample-and-hold circuit is based on the operating budget that the AWA facility has for manufacturing the BPM prototype signal detector and signal processing boards. The central idea is to have all frequency components of the elongated BPM signal to lie within the frequency bandwidth of the SAH circuit so that it can successfully track the signal in an uninhibited way before latching the peak amplitude of the elongated BPM signal via an externally triggered hold operation that is issued to it.

As stated previously, simulation of the BPM signal-detector prototype board was done throughout the course of the design and testing of the BPM prototype system utilizing the simulation software tools LTspice and QUCS. LTspice is freely distributed by the electronics company Analog Devices and QUCS (Quite Universal Circuit Simulator) is freely distributed as a GNU-based software package. Both simulation tools have a wide variety of linear and non-linear lumped components that can be incorporated into schematic diagrams for transient analysis and/or AC or DC frequency sweep analysis. For the BPM signal detector prototype board, the lumped components were modeled in accordance with how the circuit was designed in the finalized KiCad hardware schematic diagram. Additionally, a third party model of the 2N2222 active filter transistor (see Table 7) was imported into the LTspice simulation environment so that accurate simulations of the BPM prototype signal detector board could successfully occur.
Table 7: Attributes of 2N2222 BJT Transistor Chip [50]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-base breakdown voltage</td>
<td>75V</td>
</tr>
<tr>
<td>Collector-emitter breakdown voltage</td>
<td>40V</td>
</tr>
<tr>
<td>Emitter-base breakdown voltage</td>
<td>6V</td>
</tr>
<tr>
<td>Collector cut-off current</td>
<td>10nA</td>
</tr>
<tr>
<td>Emitter cut-off current</td>
<td>10nA</td>
</tr>
<tr>
<td>Collector-emitter saturation voltage</td>
<td>0.3V</td>
</tr>
<tr>
<td>DC current gain</td>
<td>35</td>
</tr>
<tr>
<td>Transition frequency</td>
<td>300MHz</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>25pF</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>8pF</td>
</tr>
<tr>
<td>Noise figure</td>
<td>4dB</td>
</tr>
</tbody>
</table>

When doing simulation analysis of the BPM signal detector board, a standard BPM raw input signal was used that was closely modeled to the real BPM signal as generated within the linear accelerator at the AWA facility. The time stamp and magnitude information related to the signal was manually stored as a standard text file containing two columns of information: the time stamp of the input signal and the corresponding voltage magnitude of the BPM signal. The text file was then imported into LTspice or QUCS by assigning it to a voltage source component and then attaching it to the simulated BPM signal detector circuit at the place (in the schematic diagram
of the same) where the raw BPM input signal enters the board. The simulated BPM raw input signal (as used in the simulated LTspice or QUCS signal detector circuit) has a pulse width of approximately 800 picoseconds and a voltage peak amplitude of 1.10 millivolts.

From a quantitative standpoint, a key point of interest related to the sample-and-hold circuit on the BPM signal detector board is its small-signal bandwidth. For the AD783 sample-and-hold chip, the small-signal bandwidth is 15MHz, which is the frequency at which, for a 100mV peak-to-peak sine wave, the signal amplitude at the output of the sample-and-hold chip is less than the signal amplitude at the input of the sample-and-hold chip by 3dB. This is an important benchmark with respect to how much the BPM input signal should be elongated in time by filtering out and/or attenuating high-frequency components via the LC filter resonator so that the remaining frequency components lie within the small-signal bandwidth of the sample-and-hold chip on the BPM signal processing board [39].

Another important quantitative part of the BPM prototype system is the signaling components that synchronize and time when the sample-and-hold and analog-to-digital conversion operations occur. These operations have to be carefully timed so that the hold operation on the sample-and-hold circuit is triggered precisely at the point when the peak magnitude of the BPM filtered signal is being tracked by it on the BPM signal processing board. Likewise, the timing and initiation of the start conversion operation on the analog-to-digital converter chip must also be carefully synchronized by the timing and signaling hardware components on the BPM signal processing board.
CHAPTER 5
RESULTS

Section 5.1 : Bench Testing Results

The first thing done with respect to bench testing the BPM signal detector board was to test it in an environment where no input signal was fed to it from an external source of any kind. The purpose for this type of testing configuration was to determine whether any forms of noise internal to the BPM signal detector itself were passing through the active filter in a powered-up steady-state mode of operation. The apparatus used for this form of bench-testing simply consisted of the BPM signal-detector board attached to an external 12-volt power supply and a matched 50-ohm BNC coaxial cable connected to an external oscilloscope from the output of the third-stage active filter on the signal detector board [51].

As displayed in Figure 30, it was observed that a form of persistent steady-state noise was present at the output of the third-stage of the active filter after the BPM signal detector board was powered up. The voltage level of the noise-burst signal was measured on the oscilloscope and found to be in the approximate range of 20mV. It was later determined after further investigation that the source of the persistent noise was in all likelihood from the periodic switching operations that were occurring in the AC-DC power converter on the BPM signal detector board. It was then
determined to insert a LC low-pass filter between the 12-volt power supply and the first-stage of the active filter that attenuated, (as seen in Figure 30), the unwanted noise-burst signal to approximately 1mV and prevented it from passing through the active filter [51].

![Image](image1.png)

a) with noise-burst b) noise-burst removed (via LC lowpass filter)

Figure 30: BPM bench testing results (active filter with no input signal) [51].

A bench test then followed that had to do with generating a single-shot pulse of fixed duration such that the incoming BPM raw signal could be simulated using an off-the-shelf waveform generator attached to the BPM signal detector prototype board. For this series of tests, a model Quantum 9530 model signal generator was used to generate the single-shot pulse. The pulse width of the signal generated for this series of bench tests was 2-nanoseconds and corresponded to the shortest pulse width available to generate using the 9530 signal generator. The signal from the 9530 signal generator was then fed into the active filter input on the BPM signal detector board using a standard BNC coaxial cable [51].
There were then several measurements made using the 9530 signal generator to generate the 2-nanosecond width pulse and having various levels of peak amplitude. The main purpose for varying the peak amplitude of the single-shot pulse was to see whether the corresponding active filter response on the BPM signal detector board was in direct proportion to the magnitude of the input signal coming from the attached 9530 signal generator board. Upon further inspection, and using an oscilloscope attached to the output of the active filter on the BPM signal detector board, it was confirmed that the magnitude of the filtered and amplified signal was in one-to-one direct proportion to the magnitude of the simulated BPM signal coming from the 9530 signal generator board [51].

In order to accomplish attenuation of the simulated BPM input signal originating from the 9530 signal generator, a third-party off-the-shelf hardware attenuator module was attached between the signal detector board and the BNC cable connected between the signal generator and signal detector board. For the experiment, there were a total of three separate unipolar input signals that were generated, each having a 2-nanosecond pulse width. Due to the use of the BNC cable, the signal from the signal generator was inverted and at the input of the BPM signal detector board, had a full-width-at-half-maximum (FWHM) pulse width of 10 nanoseconds and peak magnitude of approximately -125mV. The corresponding active filter output was then measured with an oscilloscope attached to it (and as displayed in Figure 31 and Table 8), had a peak amplitude of approximately 130mV and a FWHM pulse width of approximately 500 nanoseconds. The second input signal generated was intentionally attenuated and had a peak amplitude of about -50mV as measured at the input of the active filter on the signal detector board. As seen in Figure 31 and Table 8, the corresponding voltage, as measured at the output of the active filter, was
approximately 55mV and a FWHM pulse width of approximately 500 nanoseconds. The third (attenuated) input signal had a peak amplitude of about -16mV as measured at the input of the active filter on the signal detector board and had a corresponding output voltage at the active filter output, as seen in Figure 31, of approximately 20mV and a FWHM pulse width of approximately 500 nanoseconds [51].

Vin= -125mV        Vin = -50mV        Vin= -16mV
Vout=130mV          Vout = 55mV       Vout = 20mV

Figure 31: BPM bench testing results (active filter excited by input signals of various peak magnitudes) [51].
Simulation results of the BPM signal detector board included a series of tests in LTspice where the incoming BPM raw signal was scaled in magnitude to simulate various charge levels that a charge beam can have when it is accelerated in the particle accelerator and detected by a BPM button electrode. The scaling of input magnitude of the raw BPM incoming signal was to determine whether the relationship that existed between its peak magnitude and the peak magnitude of the output response of the active filter was linear in nature or had at least a one-to-one uniqueness property to it. Another important outcome to measure in the simulation testing of
the BPM signal detector board was the pulse width of the elongated BPM signal as measured at the output of the active filter.

An amplitude scaling simulation test first involved exciting the BPM signal detector active filter with an unscaled BPM raw input signal and then measuring the peak magnitude of the elongated signal at the output of the active filter. For this series of simulation tests, the peak amplitude of the unscaled BPM input signal was 1 volt (Figure 32). As seen in Figure 33, the peak magnitude of the elongated signal at the active filter output was found to be approximately 30 volts. The active filter was then excited with a raw BPM input signal scaled by a factor of 0.1 and the peak magnitude of the elongated signal at the active filter output was found to be approximately 2.5 volts. Similar simulation tests that involved exciting the active filter with a raw BPM input signal with scaling factors of 0.01 and 0.001 produced an elongated signal at the active filter output having respective peak amplitudes of approximately 0.2 and 0.02 volts. For each experiment of scaling the raw BPM input signal, the pulse width of the corresponding elongated signal at the active filter output was approximately 500 nanoseconds. As seen in Table 9, the LTspice simulation test results are supportive of linearity between the input and output peak magnitudes of input and output signals of the BPM RFFE board [47].
Figure 32: BPM (unscaled) input signal used for BPM active filter simulation testing.

BPM output signal (using a BPM input signal with scaled peak-amplitude of 1.0V)

BPM output signal (using a BPM input signal having a scaled peak amplitude of 0.1V)

BPM output signal (using a BPM input signal having a scaled peak amplitude of 0.01V)

BPM output signal (using a BPM input signal having a scaled peak amplitude of 0.001V)

Figure 33: BPM active filter simulation results (prototype RFFE board) [47].
Table 9: BPM Active Filter Simulation Testing Results

<table>
<thead>
<tr>
<th>BPM input voltage signal (peak amplitude)</th>
<th>BPM output voltage signal (peak amplitude)</th>
<th>FWHM pulse width</th>
</tr>
</thead>
<tbody>
<tr>
<td>~1V</td>
<td>~30V</td>
<td>500 ns</td>
</tr>
<tr>
<td>~100mV</td>
<td>~2.5V</td>
<td>500 ns</td>
</tr>
<tr>
<td>~10mV</td>
<td>~0.2V</td>
<td>500 ns</td>
</tr>
<tr>
<td>~1mV</td>
<td>~0.02V</td>
<td>500 ns</td>
</tr>
</tbody>
</table>

Section 5.3: Target System Results

The initial testing of the BPM signal detector prototype board on the target system at the AWA facility was divided into three separate experiments consisting of noise-floor test, medium beam-charge test, and low beam-charge test. For these experiments, a strip-line pickup was used to detect the accelerated charge beam and transmit the induced BPM signal to the signal detector board. For the first experiment, the signal detector board was enclosed within the bunker of the particle accelerator itself but without it being connected to the nearby electrode pickup that was mounted inside the accelerator beam-pipe walls. Measurements of the voltage at the active filter...
output of the signal detector board were then made as accelerated charged particles passed by its immediate vicinity within the nearby beam-pipe walls. The reason for this configuration was to determine whether any noise generated in the immediate vicinity of the signal detector board from the accelerator itself was passing through the input of the active filter and getting amplified as seen from the output of the active filter. The second experiment was to accelerate a medium-level beam of charges and then, with the nearby electrode pickup attached to the signal detector board, measure the corresponding voltage at the output of the active filter [51]. The induced voltage is the result of electro-magnetic coupling between the accelerated charged particles and attached electrode pickup embedded within the beam-pipe of the particle accelerator walls [23]. The third experiment was to then incrementally decrease the beam charge level and measure the corresponding voltage at the active filter output until a signal that can be measured no longer appears. This will then establish the low-end sensitivity range of the BPM signal detector board [51].

The results of the first test revealed that there was no discernable signal present at the output of the active filter on the signal detector board. This was a desired outcome in that it revealed that no noise-generated signals were passing through the active filter for amplification in the real-world external environment of the signal detector board running within the particle accelerator itself. As displayed in Figure 34, the results of the second test revealed that for an approximate 0.5 nano-coulomb accelerated charge beam, the response of the active filter was a signal having a pulse width of approximately 20 nanoseconds and a peak magnitude of approximately 100 millivolts. The results of the third test revealed that using an oscilloscope connected to the output of the active filter on the signal detector board, no discernable signal was
present for a bunch charge level immediately below the 0.5 nano-coulomb bunch charge level from the previous experiment. The 0.5 nano-coulomb bunch charge level of the previous experiment then established a lower limit to the input sensitivity of the signal detector board while running in the target environment of the particle accelerator itself [51].

The target system testing of the prototype signal detector board using a BPM button pickup did not produce any meaningful results when attempting to measure an incoming BPM signal from a charge beam having a roughly 0.5 nC charge [52]. Another target system test some months later at the AWA facility was done using a modified prototype signal detector board where the footprint lead traces on the PCB board for the 2n2222 transistor were corrected and resulted in more promising results. As seen in Figure 34 and Table 10, the output response of the active filter to a charge beam having a 2nC charge had a peak amplitude of 3mV and a FWHM pulse width of approximately 3.5 micro-seconds. No further measurements for beam charge levels were made due to the fact that the peak amplitude of elongated output signal was at an already lower range, indicating that it would be too small for any beam charge levels below the mid-range charge level of 2nC previously measured [53].
Figure 34: BPM target system testing results [51, 53].

Table 10: BPM Active Filter Target System Testing Results

<table>
<thead>
<tr>
<th>BPM input voltage signal (peak amplitude)</th>
<th>BPM output voltage signal (peak amplitude)</th>
<th>FWHM pulse width</th>
<th>Type of BPM pickup</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5nC -&gt;~ 15V</td>
<td>~100mV</td>
<td>20ns</td>
<td>stripline</td>
</tr>
<tr>
<td>100pc -&gt;~ 3V</td>
<td>0mV</td>
<td>N/A</td>
<td>stripline</td>
</tr>
<tr>
<td>2nC -&gt;~ 6V</td>
<td>~3mV</td>
<td>3.5us</td>
<td>button</td>
</tr>
</tbody>
</table>
Chapter 6

Conclusion and Future Work

Section 6.1: Conclusions

The bench testing results of the BPM signal detector active filter reveal that for the three input signals generated, the pulse width of each corresponding output signal (approximately 500 nanoseconds) fits well within the 15 MHz small-signal bandwidth of the sample-and-hold circuit on the BPM signal detector board. This was determined by taking the inverse of the output pulse-width of 500 nanoseconds, which is 2 MHz. The inverse value can be seen as representing the spectral content of the main lobe in the frequency spectrum of the BPM active filter output signal. As such, the preliminary bench test results indicate that the bandwidth of the BPM active filter output signal is within an acceptable range of the sample-and-hold circuit’s frequency bandwidth.

Another attribute of interest in the BPM bench testing data results is that the magnitude of the active filter output signal was in one-to-one direct proportion to the magnitude of the BPM input signal into the active filter on the signal detector board. Having a relationship between the input and output signals of the active filter that is proportional in nature ensues that the position information of the charged beam can be successfully extrapolated by having a one-to-one mapping
between the input and output active filter signals via a constant of proportionality (if linearly related) or via some form of calibration done beforehand where a unique mapping of input magnitudes to output magnitudes of the active filter can be firmly established.

Another attribute of interest to be noted from the bench-testing results was that the FWHM pulse width of the active filter output signal for each experiment remained the same at approximately 500 nanoseconds. These results indicate that the rise-time values of the same signals are also the same as well. This is a critical finding in that the timing circuitry design on the BPM signal processing board will work correctly only when the rise-time of an output signal of the BPM active filter always remains the same regardless of its peak amplitude. The timing circuitry on the signal detector board effectively starts a timer once the zero-crossing of the active filter output signal is detected (in accordance with the frequency bandwidth of the AD8611 comparator circuit) on the BPM signal processing board.

The results of BPM signal detector board running on the target system of the particle accelerator (using strip-line electrodes) revealed that the active filter produced promising results for input signals having voltage levels that correspond to beam bunchs having a charge level of approximately 0.5 nC. The pulse width and height of the active filter’s output response was within acceptable range for downstream components to properly process via track and hold operations of the sample-and-hold circuit on the signal processing board. However, due to the active filter’s inability to produce any meaningful output below voltage level corresponding to 0.5 nano-coulombs, the sensitivity of the active filter to detect and/or amplify incoming BPM signals that correspond to beam charge levels in pico-coulomb range is unsatisfactory in scope and degree.
Section 6.2: Discussion and Future Work

The BPM prototype RFFE board, under target testing conditions at the AWA facility (using button electrodes), was able to produce positive results including the elongation and amplification of the incoming BPM signal at charge levels of the beam bunch in the approximate range of 1-2 nano-coulombs. For charge levels in pico-coulomb range, it was unable to produce results at the output of the active filter that were discernable to measure, so it was unable to meet the dynamic range requirement into the pico-coulomb range. One reason for the BPM prototype RFFE board not having the proper sensitivity to the BPM incoming signal could be related to unaccounted for capacitive parasitic effects of the active filter (between the leads of the transistor and between its internal junctions) for frequencies in the several MHz or GHz range. The transition frequency of the 2n2222 transistor (300 MHz) was also most likely causing it to act as a low-pass filter for higher frequency contents beyond the several hundreds of MHz range. Another mitigating factor that could have contributed to the adverse performance of the BPM prototype board was that the software used to simulate its operation under target system conditions most likely didn’t fully model the parasitic effects on it when conditioning the incoming BPM pulsed-RF signal.

As a way to resolve some of these issues, it would perhaps be helpful to build the parasitic components (as elaborated on in [32] and in Figure 16) into the simulation model used in LTspice or other simulation software so as to compare the target system results with those produced in the simulation until an agreement in measurement between the two (at the output of the active filter) is fully met. As stated in [54, 55], all single lumped-component elements begin to function as RLC
combined components past approximately 10MHz, so explicitly building the equivalent model into the circuit being simulated could identify potential pitfalls in design for signals with frequency components beyond the 10MHz range. As stated in [32], the parasitic effects inherent in the through-hole leads of the BJT transistor at high frequencies might make using surface-mount transistors a better choice. As stated in [32], inverting transistors at high frequencies are more susceptible to the Miller Effect, so a non-inverting transistor might mitigate those effects at higher frequencies within the BPM pulsed-RF signal. As stated in [54], a lumped component and PCB design method works up to approximately 10 GHz in incoming frequency, so the present method of circuit implementation could be used, but with RF-based lumped components that are specifically designed to operate within those ranges of frequencies.

Another more likely explanation for the BPM prototype RFFE board not having full sensitivity to the BPM input signal at lower charge levels is due to the energy level of the signal. This level is in the frequency band of the LC resonator on the BPM prototype board, which is 1.59MHz. In the frequency spectrum of the BPM input signal (see Figure 7), the energy contained in the 1.59MHz can be much closer to the noise floor of the RFFE board for charge levels that are in the mid to lower-pico-coulomb range. It was also later discovered that the LTspice simulator used for simulation testing of the BPM prototype RFFE board does not simulate thermal noise of components when transient analysis experiments on the circuit were being done [56].

Another contributing factor to this explanation (weaker energy level in 1.59MHz frequency band of LC resonator) is that the high-frequency components of the BPM signal are attenuated by 40dB per decade by the second-order LC resonator. This leads to having their contribution to the overall signal amplitude of the resonator’s output response to become less with
increasing frequency. The peak energy of the BPM input signal (i.e., 1.5GHz) is therefore considerably attenuated to where its overall contribution to the magnitude of the elongated BPM signal (in the time domain) is negligibly small. This would also be the case of the high-frequency components of the BPM input that are parasitically attenuated in the RFFE board. This is largely due to the capacitive parasitic effects that are inherently operative on the BPM input signal frequency components that are in the higher (GHz) frequency range.

One proposed method of RFFE design is to continue the method of narrowband processing of the BPM input signal but to bandpass filter the signal in the frequency range with the greatest energy (i.e., for AWA facility, 1.5 GHz). This would have the benefit of attaining the highest signal-to-noise ratio before filtering the signal and is an especially critical outcome for beam charge levels that are in the mid or lower pico-coulomb range. This form of RFFE implementation would require an RF mixer, local oscillator (LO) and phased-lock loop (PLL), and/or voltage-controlled oscillator (VCO) circuit components. This form of implementation would also need to fully account for parasitic effects in the RFFE design due to the BPM input signal’s frequency band of interest being in the 1.5GHz range. Frequency components of the BPM input signal in this range can be more impacted by the parasitic effects inherent in the passive and lumped-circuit components used in the design. The parasitic effects can be mitigated by using commercial off-the-shelf (COTS) surface-mount RF lumped components such as low-noise and narrowband (i.e., tuned) amplifiers specifically designed to operate in the GHz frequency range. In this form of RFFE implementation, impedance matching to eliminate signal reflections from occurring between interconnected RF lumped components is also an important part of the overall circuit design.
Another method of narrowband processing for the BPM prototype RFFE circuit would be to continue to utilize the 1.5MHz frequency band (or comparable lower frequency band) as the frequency band of interest in bandpass filtering. However, a thorough analysis would be needed on the various forms of noise and signal loss externally or internally present in or inherent to the BPM prototype RFFE system (thermal, shot, RF, Gaussian noise, cable attenuation) at the frequency range of interest. Also, one needs to identify the frequency spectrum of each noise or signal-loss source, especially as it relates to the lower frequency band (i.e., 1.5MHz) of interest, where overlapping noise and BPM input signal frequency components could potentially occur. This could then establish a signal-to-noise ratio benchmark to more carefully consider, especially for the case of BPM charge levels that are in the mid to lower pico-coulomb range.

For this method of implementation, further consideration could be given to the BPM button pickup that acts as a first-order highpass filter (see Figure 6) to the BPM prototype RFFE board. The cutoff frequency to the filter is typically in the several hundred MHz range [24]. This means that the incoming BPM signal in the 1.59MHz range is being attenuated. To prevent the attenuation, the cutoff frequency of the button pickup high-pass filter needs to be lowered by either increasing the input impedance (see Figure 4) of the BPM prototype RFFE board or to increase the capacitance of the BPM button pickup itself. This would then prevent the 1.5MHz frequency from being attenuated by moving the cutoff frequency of the button pickup high-pass filter closer to kHz or lower range. In such an endeavor, increasing the input impedance of the BPM prototype RFFE board would result in a substantial impedance mismatch with the 50Ω coaxial cable it is attached to, so seeking to increase the capacitance of the BPM button pickup itself might be a more promising option to pursue.
A method of using the first-stage transistor of the BPM prototype RFFE board to clip the raw BPM input signal (by biasing the transistor to operate in cutoff mode for the negatively valued portion of the BPM bipolar signal) has been conceived and explored by the AWA facility to allow for continued use of the near-MHz frequency range with promising results [57]. For their tests, they created an updated RFFE design utilizing a 2SC4083 bipolar transistor. While in cutoff mode, the transistor generated harmonics from the clipping operation that also resided in the near-MHz frequency band of interest. These harmonics therefore contributed to the total energy in that frequency band. Initial tests also indicated that the harmonics generated from the clipping operation were in proportion to the peak magnitude of the BPM input signal. As a result, this can be a way to prospectively generate new energy in the near-MHz frequency band that was otherwise lacking in the raw BPM input signal, and that improves the signal-to-noise ratio in that frequency band for later stages of amplification and filtering on the redesigned BPM prototype RFFE board.

The current BPM prototype board does not have a built-in transmission line to match impedance with the characteristic impedance of the coaxial cable, so reflections are to some degree occurring for BPM signals incident upon it. The signal-loss or added-noise figure generated from the reflected signal may be something that needs to be investigated further. With all engineering endeavors, there is a trade-off design-wise between one desirable outcome and one that is less desired. As stated in [58], the broadband nature of the BPM pulsed-RF signal may mean that achieving matched impedance may be at the loss of input dynamic range and/or increased noise figure for the RFFE board. An alternative approach would be to do impedance matching only for the frequency band of interest and to allow reflections to occur for frequency components of the BPM input signal that lie outside the frequency band of interest for later bandpass filtering. RF
impedance-matching components are sold at reasonable cost that allow for frequency-band
impedance matching to $50\Omega$. Thus, this is an option that could be further explored as well.

As described in [8], a cost-saving endeavor in RFFE design could be to use a delay line
and broadband combiner to serially route two separate BPM signals, as received from two separate
BPM electrode pickups, into one BPM prototype RFFE board. This would then permit processing
of each BPM button pickup signal to serially occur using one RFFE board instead of processing
each BPM button pickup signal in parallel using two or four separate BPM prototype RFFE boards.
The method of processing multiple BPM button pickup signals serially using one RFFE board
would then be indistinguishable from processing a pulse train of BPM signals from a single button
pickup. The low repetition rate (2Hz) at the AWA facility for incoming BPM signal could allow
this method of RFFE implementation to be more fully explored.

As described in [11], connecting a narrow bandpass filter and/or low-noise amplifier
directly to the BPM button pickup itself may offer promising results with respect to preventing
the BPM pulsed-RF signal from being submerged in downstream noise for beam bunches that have
lower charge levels, especially in the lower pico-coulomb range. Upon implementation of the
feature, additional testing at the AWA facility could prospectively confirm whether improved
signal-to-noise ratio of the BPM signal into the prototype RFFE board afterward occurs.

As described in [2] and [3], an alternate solution might be to have minimal analog
components to the BPM prototype RFFE board and instead route the incoming BPM pulsed-RF
signal directly into an ultra-fast RF analog-to-digital converter (having sampling rates in the GHz
range) so that digitization of the signal can immediately occur. This is typically done by bandpass
filtering the input signal in the frequency band of greatest energy (for the AWA facility particle
accelerator, 1.5GHz). This is followed by digitizing the filter’s output response by bandpass sampling it [14] via a high-speed RF analog-to-digital converter that is connected to it. The cost of such components is now more affordable to obtain, and the act of immediate conversion of the RF signal into digital form eliminates the parasitic effects that would otherwise be present when implementing a traditional analog RFFE receiver to condition and transform the incoming BPM raw signal from the BPM button pickup.

At the present time, the AWA facility has made modifications to the BPM prototype RFFE board by using a two-stage active filter and (as seen in Table 11) a 2SC4083 RF-based transistor having a higher transition frequency ($f_T = 3.2GHz$) than the 2n2222 transistor that was on the BPM 2n2222 prototype RFFE board [53]. Initial target system testing was recently done and showed that the new RFFE board was able to detect beam bunches with charge levels as low as 150 pico-coulombs. There has also been consideration of possibly modifying one of the previous BPM prototype designs utilizing a standard high-speed peak detector so that it is more similar to the design as described in [8]. For that design, a Schottky diode was implemented in the RFFE for its greater sensitivity to the input signal’s dynamic range. The Schottky diode also has less reversed-biased capacitance, so it is able to operate more effectively at frequencies in the GHz range [59].
Table 11: Attributes of 2SC4083 BJT transistor chip [60]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-base breakdown voltage</td>
<td>20V</td>
</tr>
<tr>
<td>Collector-emitter breakdown voltage</td>
<td>11V</td>
</tr>
<tr>
<td>Emitter-base breakdown voltage</td>
<td>3V</td>
</tr>
<tr>
<td>Collector cut-off current</td>
<td>500nA</td>
</tr>
<tr>
<td>Emitter cut-off current</td>
<td>500nA</td>
</tr>
<tr>
<td>Collector-emitter saturation voltage</td>
<td>0.5V</td>
</tr>
<tr>
<td>DC current gain</td>
<td>56</td>
</tr>
<tr>
<td>Transition frequency</td>
<td>3.2GHz</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>0.8pF</td>
</tr>
<tr>
<td>Noise figure</td>
<td>3.5dB</td>
</tr>
</tbody>
</table>
REFERENCES


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