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Extended "A Comprehensive and Unified Procedure for Symbolic Analysis of Analog Circuits"

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***abstract*— The objective here is to expand and complete the development of a recently published article "A Comprehensive and Unified Procedure for Symbolic Analysis of Linear Analog Circuits". This expansion is in three areas. 1) Here, the element values are not limited to admittances. Both admittances and impedances are used. 2) The linear active devises are not limited to VCCSs, but the other controlled sources, VCVSs, CCVSs, and CCCSs are also valid components. 3) The I/O ports are expanded and now all four types of I/O ports, namely, current source inputs and voltage outputs, current source inputs and current outputs, voltage source inputs and voltage outputs, and voltage source inputs and current outputs are included in the process.**

The method consists of two main processes. In the first process a circuit with active devices and I/O ports is converted into a nullor circuit. The nullor circuit is then partitioned into two parts, a passive circuit and an all-nullor circuit. It is shown that the magnitude of the determinant comes from the passive part and the sign (0, 1, or -1) results from the all-nullor circuit.

***Keywords*— admittance method, analog circuits, parallel-series operations, sum of tree products, transfer functions**

I. Introduction

Finding circuit transfer functions, whether numerically or symbolic through topological formula is originated from Binet-Cauchy Theorem [1] for passive circuits. The formula is based on the circuit tree-enumeration, known as Sum of the Tree-admittance Products (STP). Many modifications and developments have been happening particularly for active circuits [1 - 7], and the focus has been on the efficiency and the computational time [8 - 15]. With all the developments being done still certain problems remain unresolved. For example, to go for tree enumeration we need to deal with the entire circuit multiple times. Partitioning the circuit is of course possible but the parts grow almost exponentially adding to the process time. Other problems are, for instance, 2-graph requirement for active circuits, as well as, 2-trees constructions are needed to find cofactors and ultimately the I/O transfer functions.

In a recent article, "A Comprehensive and Unified Procedure for Symbolic Analysis of Analog Circuits" published in TCAS-I [16] some of the major problems in STP methodology has been resolved. There are two major developments reported, 1) use of the Admittance Method (AM), and 2) the nullor circuits replacing the controlled sources as well as I/O ports. In AM, the passive portion of a circuit is reduces gradually to a single element, representing the circuit determinant and cofactors. On the other hand, the active portion of the circuit plus its I/O ports are replaced with nullors, all represented in a nullor circuit. As we notice, there is no mention of 2-graphs or 2-trees here.

With all the advancement being done in [16], however, still there are three types of short comings that are present, which limit its application in a general active circuit. The article [16] tries to find a transfer function of a linear active circuit containing VCCSs and nullors. The I/O ports also need to be of the input current source and the output voltage type. Finally, the circuit elements need to be of admittance types only. This is, of course, consistent with the Nodal Admittance Matrix (NAM), where the circuit values are admittance (g_m and y) based as well.

The objective in the current presentation, however, is to eliminate those limitations and make the methodology open and general to work with other depending sources as well as with other I/O types. The changes in these new developments are as follows.

1- The passive components are given in both admittance and impedance terms. This is possible because, as discussed in [8 and 16], admittance y_i is represented by $y_i = n_i/d_i$, hence it can be simply turned into impedance $z_i = d_i/n_i$. Therefore, the data type here is more general and not limited only to admittances.

2- The second limitation that is removed in this presentation is the exclusive use of VCCSs as the only active component. Here, we can have any type of control source, namely VCVS, VCCS, CCVS, or CCCS with no need to convert them to VCCS. In fact, mixing all types of controlled sources are permitted here, as Example 2 shows.

3. As we mentioned before, the I/O ports in [16] are limited to current inputs and voltage outputs (CIVO). This is also of admittance type and suitable to include them in the NAM, just like VCCSs. What we need here is to include the other types of I/O ports, namely, voltage inputs and voltage outputs (VIVO), current inputs and current outputs (CICO), and voltage inputs and current outputs (VICO), which collectively cover all types of I/O ports.

The paper is organized as follows. Section II is a review of the Admittance Method (AM), originally covered in [8 and 16]. Section III is about Nullor Circuits and the use of AM in nullor circuits. In Section IV AM is generalized including all four types of controlled sources and four types of I/O ports. Two circuit examples are worked out in this section that show how the Admittance Method is applied to the most generalized circuits with different types of dependent sources and I/O ports. Brief discussions about pathological elements and reactive components are also included in Section IV. Section V is Conclusion. Finally, it is important to note that, the STP procedure in only applicable to linear circuits and not to large-scale circuits.

II. Admittance Method - A Review

Admittance Method is fully discussed in [8 and 16], and here we make a short review of the subject.

In a linear circuit N with a pair of I/O ports i and j, the transfer function $p_{ji}(s)$ can be written as

$$p_{ji}(s) = T / T_{ji} \qquad (1)$$

where, T and T_{ji} denote the determinant and the ji cofactor of the circuit computed through STP operations. Equation (1) also applies to the admittance of a single or multiple combinations of connected elements. For example, the admittance of an element e_i, is written as $y_i = n_i/d_i$, where n_i, and d_i are the determinant and a cofactor of e_i,, and d_i is *1* for a single element. Evidently the impedance z_i or r_i can be written as $z_i = d_i/n_i$.

Now, we may apply certain admittance operations on passive components in a connected circuit, which is called *Admittance Method (*AM*)*.

Given a passive circuit N, the AM is used to reduce N into a 2-terminal component with admittance $y_t = n_t/d_t$, where $n_t = T$ is the determinant (STP) of N and d_t is a cofactor of N. In each step of an AM operation one of the following three *basic* procedures is applied to N: a) *parallel*, b) *series*, or c) *partition*.

Parallel and Series – For two parallel admittances $y_i = n_i/d_i$ and $y_j = n_j/d_j$ we get the replacement admittance y_p as

$$y_p = \frac{n_i d_j + n_j d_i}{d_i d_j} = \frac{n_i d_j}{d_i d_j} + \frac{n_j d_i}{d_i d_j} \quad (2)$$

Likewise, two admittances y_i and y_j in series can be replaced with y_s as

$$y_s = \frac{n_i n_j}{n_i d_j + n_j d_i}. \quad (3)$$

When a sequence of *parallel/series (P/S)* operations is exhausted the circuit remained is a *P/S free* circuit.

Partition – When a circuit becomes P/S free, only a partition can break it and produce further P/S operations. A partition $N\{A; B\}$ is obtained from a circuit N by removing elements A and short circuiting elements B in N, and $T\{A; B\}$ refers to the determinant (STP) of $N\{A; B\}$. Now, consider a circuit N with determinant T. If N is partitioned through an element $y_i = n_i/d_i$ then we can write [16]

$$T = n_i T\{0; e_i\} + d_i T\{e_i; 0\} \quad (4)$$

As it is shown in [8 and 16], by multiple applications of AM operations the passive portion of an active circuit is totally removed, resulting in a coefficient that represents the passive determinant of the circuit. The remaining circuit contains all active devices and I/O ports, which are later converted into an *all-nullor* circuit. Therefore, to understand the entire process of getting determinants and cofactors it remains to understand nullor circuits, as stated in [16].

III. NULLOR CIRCUITS AND ADMITTANCE METHOD

A *nullor circuit* contains passive components and nullors. An *all-nullor circuit* contains all nullors with no passive element. An all-nullor circuit consists of a *nullator network* and a *norator network* combined. As shown in [16], each active device (VCCS) and each pair of I/O ports (input current and output voltage type) can be replaced with a directed nullor. Therefore, for active and I/O portion of an active circuit we only deal with nullors, and hence, any active circuit with VCCSs, I/Os, and nullors can be replaced with a uniform nullor circuit.

Uniformity – To find a (numerical or symbolic) transfer function of a linear active circuit N, which contains dependent sources, nullors, and I/O ports, we only need to construct a single nullor circuit N_n, as described below.

1. Replace all active devices (VCCSs) with nullors.
2. For each pair of I/O ports, i.e., an input current source and an output voltage port, in N remove the input current source and instead add a nullor to the I/O port (nullator at source and norator at output).

Now that we have introduced and applied nullors in active circuits, we now generalize the AM operations to include nullors as well.

Admittance Method for Nullor Circuits – Suppose N_n is a nullor circuit resulted from an active circuit N as described. We apply two separate operations to N_n, 1) The AM operations applied to the passive components of N_n, and 2) operating on the all-nullor circuit that is resulted from N_n after we are done with the passive elements.

We have already discussed the first part, applying the AM operations to the passive part until we reach to a final 2-terminal component with admittance $y_p = n_p/d_p$, where $n_p = T_p$ representing the determinant of the passive circuit. In the second step, we need to find the STP, T_n, of the all-nullor circuit and then the final determinant of the original circuit N is found to be $T = T_p * T_n$. Hence, we only need to find T_n of the all-nullor circuit. As proven in Theorem 4 in [16], $T_n = 0$, 1 or -1. So, the problem is to find 1) the magnitude, 0 or 1, and 2) the sign, + or –, of a nullor separately.

As stated in *Theorem 5* in [16], $|T_n|$ is 1 if and only if each one of the nullator and norator networks form a single tree with no loop. Otherwise, it is zero.

Alternatively, for operational simplicity, Theorem 5 can be stated as follows:

Theorem 5a - an all-nullor circuit has $|T_n| = 1$ if and only if the total number of its nodes is equal to the total number of nullors plus one, and either 1) there is no nullator or norator loop in N_n, or 2) each node is incident to at least one nullator and one norator.

The sign of T_n is somewhat involved and the details are given in Algorithm 2 in [16].

Now we are ready to start our new developments for generalized AM.

IV. GENERALIZED ADMITTANCE METHOD

A. All Types of Active components

Now the question is, how can we directly include all dependent sources into an active circuit similar to VCCSs? To answer this question, we start with a CCCS. Figure 1(b) shows a CCCS in different stages as an active device in a circuit, a nullor equivalent, and when the active device is removed from the circuit. As we can see, the only difference between a VCCS and a CCCS in an active circuit is when the nullor is removed. In a CCCS case the norator collapses to a single node, whereas, it stays open circuited in a VCCS case. Similar procedures apply to other dependent sources, VCVSs and CCVSs, as shown in Figs. 1(a) and 1(d). For example, in case of a CCVS both nullator and norator collapse when the nullor is removed. Theorem 1 generalizes all this.

Theorem 1 – A nullor in a nullor equivalent circuit of an active circuit can represent any type of controlled source

with no restrictions. However, they behave differently when the nullor is removed. The rules are as follows: if the original controlling element is a current the norator collapses. Likewise, if the original controlled source is a voltage the nullator collapses. Otherwise, the element is left open circuited.

Proof – It is sufficient to test each case separately. When we remove a VCCS in a circuit ($g = 0$) the current source gets removed and the two nodes get open circuited. In case of a VCVS when the device is removed ($e = 0$) the controlled terminal nodes collapse. In case of a CCCS, for example, we can see it from Fig. 1(b) that the nodes n_1 and n_2 are short-circuited. Finally, in case of a CCVS both pairs of nodes, n_1 and n_2, and n_3 and n_4, get short-circuited when the device is removed.

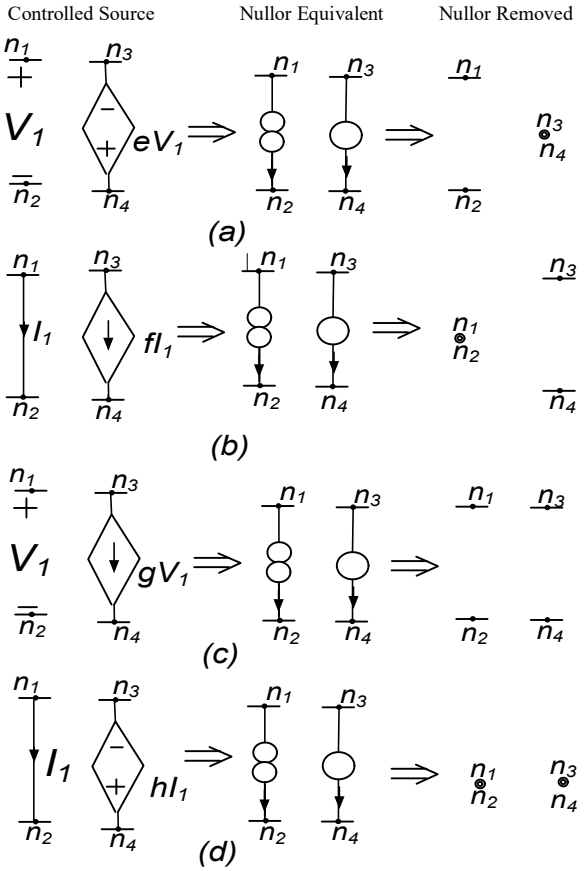

Fig. 1. Different stages of four types of controlled sources: 1) active device in a circuit, 2) a nullor equivalent, and 3) when the active device is removed from the circuit.

B. *All types of I/O ports*

According to Theorem 3 in [16], for a STP procedure, a pair of I/O ports (CIVO type) can be replace with a VCCS, and ultimately replaced with an equivalent nullor. As it turns out, the same situation applies to the other types of I/O ports, i.e., a VIVO type I/O can be replace with a VCVS, a CICO type with a CCCS, and a VICO type with a VCCS. This is symbolically shown in Fig. 2. Therefore, the nullor rules applied to the controlled sources are also one-to-one applicable to I/O ports. This bring us to Corollary 1, similar to Theorem 1.

Corollary 1 – A nullor in a nullor equivalent circuit of an active circuit can represent any type of I/O port with no distinction. However, they behave differently when the nullor is removed. The rules are as follows: if the norator denotes an output current the norator collapses. Likewise, if the original input source is a voltage the nullator collapses. Otherwise, the element is left open circuited.

The proof of Corollary 1 follows from that of Theorem 1.

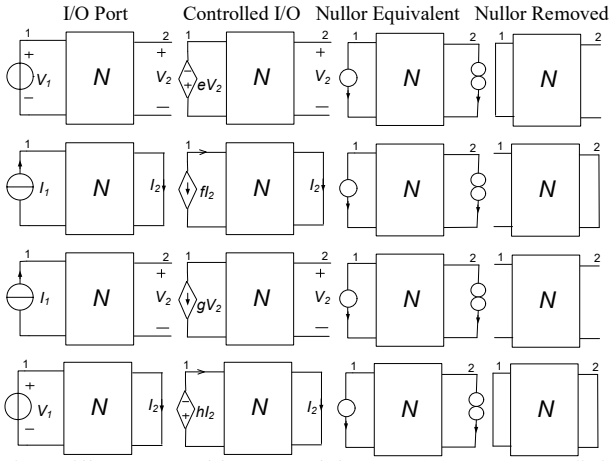

Fig. 2 Different stages of four types of I/O ports: 1) Input source applied, 2) a controlled source equivalent, 3) a nullor equivalent, and 4) when the pair of I/O ports is removed from the circuit.

Now, to test the findings we apply them to some circuits.

Example 1 – Consider the amplifier (Integrator) circuit shown in Fig. 3 (a) and its linear equivalent circuit in Fig. 3 (b) [14]. Notice that the circuit 1) has both r and y combined; 2) the active device is of VCVS type; 3) the I/O is of VIVO type. The objective here is to find the closed-loop gain of the amplifier. Figure 4 (a), provides the circuit graph including the I/O ports. To solve for the gain, we need to compute the main determinant T and the cofactor T_{21}. Two graphs, in Figs. 4 (b) and (d), are given to find T, and the other two in Figs. 4 (a) and (c) are to find T_{21}.

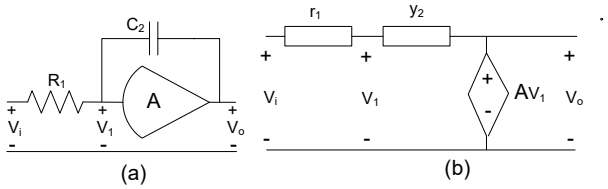

Fig. 3. An integrator; (a) circuit representation; (b) linearized equivalent circuit.

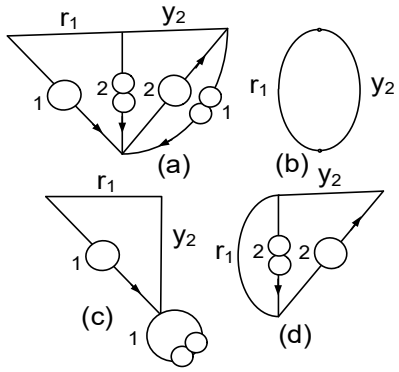

Fig. 4. Graph representation of the Integrator; (a) both active device and the I/O ports included; (b) Only passive circuit; (c) the active device removed; (d) the I/O ports removed.

For the graph of Fig. 4 (b) we can simply write

$$T^o = 1/r_1 + y_2 = (1 + r_1 y_2)/r_1 \quad (5)$$

Similarly, for the graph of Figs. 4 (d) we write

$$T^2 = -Ay_2 \quad (6)$$

and when we add them together we get

$$T = T^o + T^2 = (1 + r_1 y_2 (1 - A))/r_1 \quad (7)$$

In a similar procedure we also get

$$T_{21} = A/r_1 \quad (8)$$

from Fig. 4(a), whereas, the sub-determinant associated with Fig. 4(c) is zero. This is because of the norator self-loop. Subsequently, the closed-loop gain $A_v = T_{21}/T$ is found as

$$A_v = \frac{A}{1 + r_1 y_2 (1 - A)} = \frac{A}{1 + s r_1 c_2 (1 - A)} \quad (9)$$

Example 1 is simulated by CASD[1] and the results plus the component listing are given in Fig. 5.

```
*Amp-1 – simulator: Circuit Analysis, Simulation and Design (CASD)
r0      1       2       10
r1      3       2       50
e1      0       3       2       0       10
e2      1       0       3       0       1

Program CASD responses.
        Tmain = -40
        T21 = 500
        Av = -12.5
```

Fig. 5. Component listing and the simulation results of Example 1 using CASD tool.

Example 2 – Consider an active circuit, which is represented in its nullor equivalent graph, shown in Fig. 6. The circuit has four active components, two CCVSs (h) and two VCVSs (e), and eleven passive elements of both r and y types. The I/O ports are of VIVO type to directly provide the voltage gain A_v. The circuit is simulated using CASD tool. The component listing and the simulation results are given in Fig. 7. The SPICE result is also provided for checking purposes.

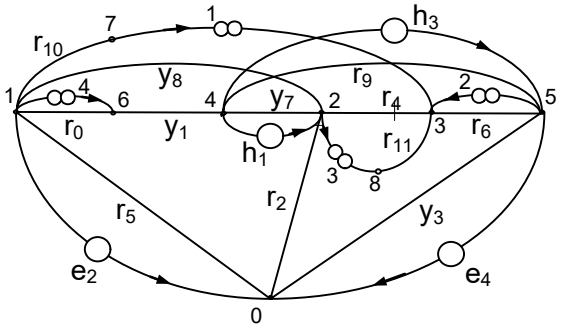

Fig. 6. A generalized active circuit represented in graph.

C. Pathological Elements

The AM works for any nullor circuit including Pathological Elements, as discussed in [16]. The difference here is that we can allow the nullors to represent different types of dependent sources as well as I/O ports. For example, Fig. 8 shows a CCII+, where the input port Y is grounded and X is excited with a voltage source, and we are asking for the output voltage, and finally the trans-impedance (trans-integrator). Notice that, while the devices nullors are of g (VCCS) type, the nullor associated with the I/O ports is of e (VCVS) type, denoting the input and output voltages.

The analysis of the circuit through STP is in two parts. First, to find the circuit determinant and then getting the cofactor for computing the trans-impedance $Z_m = V_o/I_i$, where $g_{m1} = g_{m2} = 1$. For the determinant, we need to remove the input represented by e_3 nullor. This leads to $T = sC_1 G_o$. For the cofactor e_3 nullor returns back and STP produces the cofactor $T_{oi} = -g_2$. Therefore, the trans-admittance is

$$Z_m(s) = \frac{T_{oi}}{T} = \frac{-g_2}{sC_1 G_o} = \frac{-1}{sr_2 C_1} R_o \quad (10)$$

```
*Linear active circuit – Cir2.cir - simulator: CASD
r0      6       1       2
y1      6       4       0.25
r2      2       0       4
y3      5       0       0.2
r4      2       3       5
r5      1       0       2
r6      5       3       8
y7      2       4       0.125
y8      2       1       0.25
r9      4       5       4
h1      4       2       7       3       7
h3      4       5       2       8       5
e4      5       0       1       6       3
e2      1       0       5       3       1
r10     1       7       4
r11     3       8       2

Program CASD responses
        Tmain = 1200
        T21 = -32256
        Av = -26.88

*** SPICE Simulation ***
TEMP=27 deg C
DC Operating Point ... 100%

v(5) - v(3) = -2.68800e+01
WinSpice 30 ->
```

Fig. 7 Component listing and the simulation results of Example 2 using both CASD tool and WinSpice simulator.

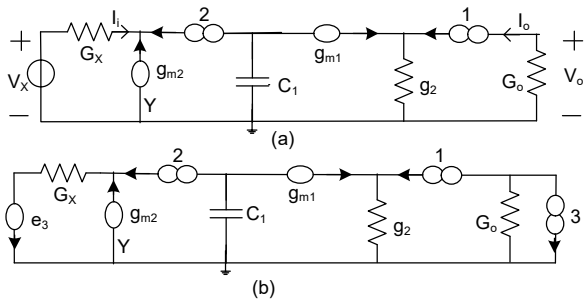

Fig. 8. (a) A nullor model of a CCII+ active device with voltage input, and (b) The CCII+ with an e (voltage in and voltage out) type nullor.

D. Circuits with reactive components (C and L)

The problem with reactive components is that they are frequency dependent. Therefore, in order to include them in an ac circuit analysis we need to use the s domain, which changes our analysis from real to complex domain. For example, the admittance of a capacitor $C_1 = 2\ \mu F$ is going to be $y_1 = 4\pi f/1$, or for an inductor $L_2 = 5\ mH$ it is $y_2 = 1/10\pi f$.

[1] The simulation program Circuit Analysis, Simulation and Design (CASD), is developed for using STP procedure to find the transfer functions in linear active circuits. The program is coded such that it can also produce the circuit parameters in symbolic format. CASD is still a domestic program, and not commercially available, pending for some publications.

Similarly, the admittance of a resistor $R_1 = 100\ \Omega$ in series with L_2 and then parallel with C_1, for f = 2 KHz, is given as.

$$y_2(s) = \frac{1 + sR_1C_1 + s^2L_2C_1}{R_1 + sL_2} = \frac{1 - 0.16\pi^2 + j0.8\pi}{100 + j20\pi} \qquad (11)$$

The same is true for other combinations of R, C, and L. As we can see, there is no difficulty in developing the admittance of combined R, C, and L circuit in s-expanded format. The same is true in developing the circuit determinant and cofactors, and finally the transfer functions. The difficulty, however, arises when we need to calculate the complex values (magnitudes and phases, for example) of a transfer function for a range of frequencies.

One way to handle this is to go through the individual frequencies and do exactly what we did for resistive circuits but in complex manipulations. This is only efficient when we have limited frequency points. A second method is to continue using AM to develop the circuit determinant and cofactors in s domain, and finally write the designated transfer function in s-expanded format. Then plug in the individual frequencies into the transfer function to evaluate the responses. Still a third option is to solve the transfer function for poles and zeros and then evaluate the responses, such as plotting the magnitudes and phases. Because of the lack of space, we refer to Example 2 in [16] for an example.

The simulator CASD uses the second option.

V. Conclution

A general and comprehensive procedure is developed for the construction of transfer functions in linear active circuits, either numerically or in symbolic form. There is no limitations in the types of components used in the circuit except for linearity. These components include all four types of control sources, and passive elements in both impedance and admittance forms. This is also applicable to I/O ports, where, the exciting input sources can be both currents and voltages. Similarly, the circuit outputs can be of both current or voltage types.

The method is based on the topological formula, computing the circuit determinants and cofactors through the Sum of the Tree-admittance Products (STP). However, for a faster computation and generalization purposes a newly developed STP technique, known as Admittance Method (AM) is utilized, which is proven very efficient in reducing the circuit to a single element with its admittance representing the circuit determinant, or a cofactor. In the present technique, all types of active devices (controlled sources) as well as I/O ports are converted into nullors. Combination of these nullors with the other passive elements produces a specific nullor circuit that carry all circuit information to the end. It is important to note that, depending on the application nullors are different. As demonstrated, there are four types of nullors for four types of controlled sources as well as four types of I/O ports, and the differences are when the nullor is removed in the circuit.

To simulate the circuit for STP operations, a program in C++, called Circuit Analysis, Simulation and Design (CASD), is developed. The simulation results of two examples are given along with the responses obtained by using the SPICE simulation. As shown, the responses completely match.

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