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A Comprehensive and Unified Procedure for Symbolic Analysis of Analog Circuits

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***Abstract*— The objective here is to develop a uniform and comprehensive procedure for symbolic analysis of linear circuits using the Sum of the Tree Products (STP) of the circuit. We achieve this goal in two stages. In the first stage a circuit with active devices, such as VCCSs and I/O ports, is changed to a nullor circuit, i.e., to a circuit with only passive components and nullors. The nullor circuit is also partitioned into two parts, a passive circuit and an all-nullor circuit. It is shown that the magnitude of the STP, i.e., the determinant of the NAM, of the circuit is equal to the STP of the passive portion of the circuit, and the sign (0, 1, or −1) of the STP comes from its all-nullor part. Another significant development in this presentation is the replacement of the regular STP methodology with a rather new Admittance Method (*AM*). It is shown that by doing this the entire two-graph theory for active circuits as well as the use of 2-tree procedures for I/O ports analysis are eliminated. It is these new developments that substantially simplifies the circuit analysis and makes it quite efficient for symbolic representation of transfer functions.**

***Index Terms*— Admittance method, analog circuits, parallel-series operations, sum of tree products, transfer functions.**

I. Introduction

SYMBOLIC representation of circuit transfer functions through topological formulas is a well-studied topic for an extended time. Different methods have been developed in the past that are challenging the subject matter further [1]–[19]. Among them, techniques such as the Sum of the Tree Products (STP) of circuits is a well-known methodology [1]–[9], [20]. Other methods such as Binary Decision Diagrams (BDD), and Determinant Decision Diagrams (DDD) are also shown to be quite effective in reducing the computational intensity [1], [3], [7]. In a similar procedure S.D. Djordjevic, P.M. Petkovicy, and V.B. Litovskiz have presented their topological oriented symbolic analysis of circuits using Topology Decision Diagram (TDD), which as stated, is inspired by the DDD methodology [21]. In another effort, S. Lasota uses Parameter Decision Diagrams (PDD), again similar to the DDD procedure, in his modeling of modern active devices [22]. Further, S. Lasota presents symbolic analysis of electric networks using PDD as well [23].

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Nevertheless, with all the progress made there have been number of generic problems that keeps these methods away from further advancements. One such problem is that, most of the methods, particularly the tree enumeration types, need to deal with the entire circuit (graph) during the operation, making it time consuming and complicated, specially for large circuits. The separation of I and V graphs, known as two-graph technique, and keeping track of the matching trees is another serious problem [1], [3], [4]. Similarly, the problem of finding and tracking 2-trees, being required for the computation of the I/O transfer functions, is another timely involvement in the process. In addition, the sign determinations in cases of the cofactors also adds another group of difficulties to the analysis of transfer functions using topological techniques. For example, as we will see, when a 4-terminal active source is broken into two 3-terminals, one appears with positive sign and the other one with negative.

Still on top of all these, is the issue of the repeated appearances of the circuit elements (branches) in multiple number of trees through the process. Due to almost exponential growth of the number of circuit trees the computational overhead payed increases very fast, making the tree enumeration methods almost impractical for large circuits. As a result, these problems has seriously hindered the practicality of the topological formulas in circuit analysis compared to the well-advanced numerical techniques.

The objective in this presentation is to further develop a technique, known as *Admittance Method (AM)* [10], for circuit analysis in order to alleviate some of the serious obstacles described, and get the topological methods applicable and efficient, at least for symbolic representation of the circuit transfer functions. Obviously, the AM procedure does not claim to effectively treat all foregoing difficulties and issues, but redirect some. First, for an optimum process, it is ideal for the operation to go through each circuit element only once. This is done through *AM* and by reducing the circuit systematically as we progress. The *AM* tries to localize the process and making the circuit continuously shrink. This is very similar to the sparse matrix analysis technique, where it concentrates on the matrix elements rather than on the complete matrix operations.

Other major steps taken in this development are the elimination of both two-graph technique for active devices as well as the 2-tree requirements for I/O transfer functions calculations. Due to the replacement of nullors for active devices, as well as the I/O ports, both two-graph and 2-tree techniques are

eliminated in the *AM* approach. Finally, the sign problem that rises from the 2-tree implementation is removed here and is replace with the nullor signs that are much simpler to formulate and resolve.

So overall, in comparing with other tree enumeration techniques and topological analysis methods reported, the AM procedure stays tall and more efficient from several respects. Those specifically include the followings. 1) Turning active circuits with VCCS devices, and I/Os into nullor circuits. 2) Gradually reducing an active circuit to a single element or to an all-nullor circuit. 3) Eliminating two-graph representation of the circuit all together. 4) Eliminating the need to use the 2-tree (or m-tree) technique for transfer function computation. 5) Finally, presenting a systematic procedure for sign determination in transfer functions calculations.

Before I conclude with this introduction, I must recognize a much similar work done by Filaretov and Gorshkov [24]. The article represents efficient generation of compact symbolic network functions in a nested rational form. They cover number of similar procedures that are presented in this submission in different forms and with no prior knowledge.

In brief, the *AM* procedure and the all-nullor circuit are two pillars of this presentation. Given a linear active circuit, the *AM* starts from any passive element and progresses toward the end, reducing the circuit through parallel and series (P/S) operations until the entire passive portion is shrunk into a single element with a total *admittance* that represents the circuit determinant/cofactor. The remaining all-nullor circuit, however, is responsible to determine the sign (0, 1, or -1) of the *admittance*. The *AM* has all the advantages of a typical STP technique with much reduced computational complexity. It is simple and fast, particularly for less populated circuits, where more series and parallel elements can be found. The *AM* procedure can also be substantially optimize by sharing certain stages of the operations between different process sections. One such optimization technique is described in Appendix A. On the other hand, in the all-nullor circuit, we first test the existence (non-zero) of thecofactor, and then the sign will emerge when we gradually remove the nullors.

This paper is organized as follows. Section II is a review of the Admittance Method [10]. It provides three basic operations that are used in the AM. Next, the AM procedure is formulated for reducing passive elements in a circuit. Section III discusses nullors and nullor circuits. Methods and techniques are provides in this section to turn an active circuit to a nullor circuit. Section IV start with a nullor circuit and operate on it until the circuit determinant or cofactor emerges. That is, the section provides the fundamental stages in dealing with nullor circuits all the way to the determination of the determinants, and cofactors with sign included. Section V discusses the AM method used in Modern Active Devices. In Section VI two circuit examples are worked out. Section VII is Conclusion. There are also Appendices A and B discussing A) an optimization method for AM operation, and B) dealing with 4-termilas VCCSs and I/Os.

II. The Admittance Method - A Review

In a linear circuit N with input and output ports i and j, the trans-admittance function can be written as

$$y_{ji}(s) = T/T_{ji} \tag{1}$$

where, T and T_{ji} denote the determinant and the ji cofactor of the NAM of N [1], [2]. Equation (1) also applies to a single or multiple combinations of connected elements. For example, the admittance of an element e_i, is written as $y_i = n_i/d_i$, with d_i starting with *1*. Similarly, two elements e_i and e_j, with the admittances $y_i = n_i/d_i$ and $y_j = n_j/d_j$ in parallel produce the admittances function

$$y_p = \frac{n_i d_j + n_j d_i}{d_i d_j} = \frac{n_i d_j}{d_i d_j} + \frac{n_j d_i}{d_i d_j}. \tag{2}$$

Also, the same elements e_i and e_j, when in series produce

$$y_s = \frac{n_i n_j}{n_i d_j + n_j d_i}. \tag{3}$$

It is important to note that, because we are dealing with determinants/cofactors no division is permitted here. For example in (2), if e_j (or e_i) is removed after the parallel operation, the resulted admittance function is reduced to

$$\frac{n_i d_j}{d_i d_j}, \quad \text{and not to the original } \frac{n_i}{d_i}.$$

Now that we understand how the admittance function of a component looks like we can describe certain admittance operations on components. Although these admittance operations work with passive components, we also need to deal with active components as well.

A. Passive Components

We start with all passive circuits and introduce the Admittance Method.

1) Admittance Method (AM): Given a passive circuit N, the *AM* is used to reduce N into a 2-terminal component with admittance $y_t = n_t/d_t$, where $n_t = T$, the determinant of the NAM of *N*. The *AM* process is a systematic process and in each step one of the following three *basic* operations is applied to N: a) *parallel*, b) *series*, or c) *partition*.

2) Parallel and Series: Two parallel components e_i and e_j with admittances $y_i = n_i/d_i$ and $y_j = n_j/d_j$ can be replace with a component e_k with admittance y_k as given in (2). Likewise, two components e_i and e_j in series can be replaced with e_s as given in (3). A sequence of *parallel/series* (P/S) operations is referred to a sequence of one or more parallel and series operations until the sequence ends up with no possible series or parallel operation in N. A circuit is P/S *free* if no more P/S operation on N is possible.

3) Partition: Given a circuit N, a partitioned circuit *N{A; B}* is obtained from N by removing elements A and short circuiting elements B, and *T{A; B}* refers to the determinant of the NAM (or STP) of *N{A; B}*. Now, consider a circuit N with its STP as T. If e_i is an element in N with $y_i = n_i/d_i$, then by applying the *partition* procedure we can write [3], [6]

$$T = n_i T\{0; e_i\} + d_i T\{e_i; 0\} \tag{4}$$

Now, suppose T^o is the determinant of the NAM of N when all of the active components are removed (open circuitrd). To compute T^o we first perform P/S operations on the circuit and reduce it to a P/S free circuit. If the circuit is terminated with a single element e_j, with the admittance $y_j = n_j/d_j$, then $T^o = n_j$. Otherwise, we make *partitioning* and remove one or more elements from N to produce P/S operations again. We continue with this process until we come up with a single element. This is not the end of the process, of course. According to (4) the process must continue with short circuiting those elements that were removed. For details refer to Algorithm 1.

Algorithm 1 To Find the Determinant of a Passive Circuit

1. Given a circuit N, perform a set of P/S operations on N first to make it P/S free.
2. Then, remove all the active components from N to make it a passive circuit N^o.
3. Again, apply P/S operations to N^o. If the result is a single element, we have done with passive circuit, otherwise the result is a P/S free circuit. Then find a node n_k with the lowest degree, say k. Remove $m = k - 2$ elements from n_k to make it a series node. Reapply P/S operations to the circuit, and in case the circuit still is not a single element continue step 3 until a single element is resulted.
4. For each element e_i removed from N^o, as a result of step 3, connect the two nodes, corresponding to e_i in N^o, together to form $N^o\{0;\ e_i\}$. Apply step 3 to $N^o\{0;\ e_i\}$ to reduce it to a single element with $n_t = T^o\{0;\ e_i\}$ as its admittance numerator. So, as the results, we have both $T^o\{e_i;\ 0\}$ and $T^o\{0;\ e_i\}$ found. The next step is to apply (4) to add up the two STPs, $T^o\{e_i;\ 0\}$ and $T^o\{0;\ e_i\}$. Continue with steps 3 and 4 until the entire circuit N^o is processed and T^o is optioned.

We are now ready to include the active components into the circuit.

B. Active Components

Up until now, we were talking about 2-terminal passive elements. For active components, we consider both 3-terminal and 4-terminal VCCSs (g_m) and I/Os. However, because of the sign determination, we need to change the 4-terminal component (if needed) to 3-terminal components. This can be done in two ways. 1) Leave them as they are until the circuit is processed and it is reduced to an all-nullor circuit, as we will discuss it later, or 2) replace each 4-terminal with two 3-terminal components.

In the first case, because all passive elements in the circuit either are removed or short-circuited the chances are that the 4-terminal components (nullors) end up becoming 3-terminals in the process. In addition, as discussed in Appendix B, the last three nullors in the STP process are becoming 3-terminals anyway. This is a strong statement, because the last three nullors can represent three 4-terminal I/Os or VCCSs.

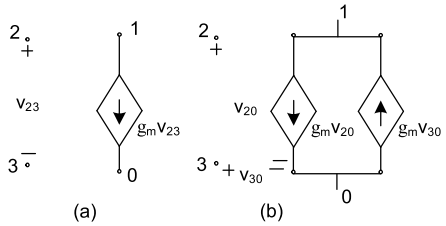


Fig. 1. Breaking a 4-nodes VCCS into two 3-nodes VCCS, where the sign from 3 to 2 is positive, but from 2 to 4 it is negative.

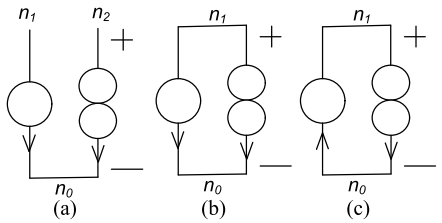


Fig. 2. Nullors; (a) three nodes, STP = 0; (b) two nodes and positive, STP = 1; (c) two nodes and negative, STP = −1.

In the second case, each 4-terminal can be replaced with two 3-terminal components, as shown in Fig. 1. However, in the process for the determination of the STP, we cannot consider the two VCCSs (nullors) present in combinations. In fact, we don't need to worry about the issue, because the two g_m make a loop, resulting in STP = 0 anyway.

Other types of active components, such as VCVS, CCVS, and CCCS, can be easily transformed into VCCSs [25].

As mentioned before, one of the major contributions of this article is the fact that the active components do not enter into the computation of the circuit determinants or STPs. They are replace with nullors, and the nullors are used only to determine the signs in the STPs. Therefore, it is sufficient to discuss circuits with only passive elements plus nullors.

III. Nullors and Nullor Circuits

A *nullor* consists of a nullator and a norator. For our purpose, we can consider two types of nullors; a) those with a common node (3-terminal), as shown in Fig. 2(a), and b) 4-terminal nullors. Like a VCCS, a 4-terminal nullor can be replaced with two 3-terminal nullors as well. Nullors also carry signs. For example, the sign of the nullors in Figs. 2(a) and (b) are positive, whereas the one in Fig. 2(c) has negative sign.

Theorem 1: Consider an active linear circuit N with one or more VCCSs. We can expand the determinant (STP) of the NAM of N in term of a VCCS, g_m, in N as

$$T = T^o + g_m T^m \tag{5}$$

where, T^o is the STP of N when g_m is removed (open circuited), and T^m is the STP of N when g_m is replaced with a nullor (the nullator replacing the controlling voltage and the norator replacing the current source).

Proof: Getting T^o is quite evident from (4). For T^m, we realize that in (5), T approaches $g_m T^m$ as g_m grows large. So, when g_m approaches infinity we can write $T = g_m T^m$.

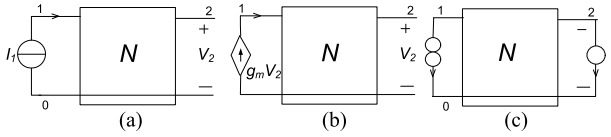


Fig. 3. A 2-port circuit to calculate the trans-conductance y_{21}; (a) the original 2-port circuit; (b) port replacement with a VCCS; (c) final replacement with a nullor.

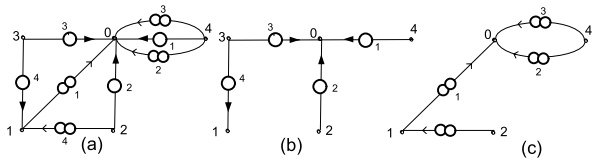


Fig. 4. (a) An all-nullor circuit, (b) the corresponding nullator network, and (c) the corresponding norator network.

On the other hand, when g_m grows to infinity the VCCS approaches to a nullor [10].

Notice that, although g_m grows in (5) as the VCCS approaches a nullor but T^m stays constant, associated with $g_m = 1$. This indicates that the magnitude of a nullor can be assumed 1. Another example is given in Fig. 2, where the STP of a single nullor is shown to be either 0, 1, or -1.

Theorem 2: Consider an active circuit N with n number of VCCSs, $g_1, g_2, \ldots, g_n$. The STP of N can be written as

$$T = T^o + g_1 T^1 + g_2 T^2 + g_1 g_2 T^{12} + g_3 T^3 + \ldots + g_1 g_2 \ldots g_n T^{12\ldots n} \quad (6)$$

where, T^o is the STP of N when all the active components are removed, and $T^{ij\ldots k}$, for all i, j, ..., and k, is equal to T when the VCCSs $g_i, g_j, \ldots$, and g_k are replaced with nullors and the rest of the VCCSs are removed from N.

Proof: The proof of Theorem 2 is quite similar to that of Theorem1, except here, instead of only one g_m, we grow all $g_i, g_j, \ldots$, and g_k to infinity and remove the rest of the VCCSs from N.

A. 2-Port Circuit

Consider a 2-port linear circuit N, shown in Fig. 3(a). We can write the transfer admittance y_{21} of N as

$$y_{21} = I_1/V_2 = T/T_{21} \quad (7)$$

where, T and T_{21} are the determinant and the trans-cofactor of N with the sign included.[1]

Next, let us remove the input source I_1 in Fig. 3(a) and instead add a VCCS with $g_m = y_{21}$ to the pair of I/O ports, as shown in Fig. 3(b). What this means is that: if we apply a voltage V_2 at the output port of the circuit, in Fig. 3(b), then the VCCS at the input port provides a current I_1 that is equivalent to the original setup (with an input source I_1). In other words, the assigned VCCS with $g_m = y_{21}$, have created a non-singularity NAM matrix with the determinant $T = 0$. So, according to Theorem 1

$$T = T - g_m T^m = 0 \quad (8)$$

Notice that, the negative sign in (8) is due to the negative sign of the VCCS in Fig. 3(b). Now, if we replace for $g_m = y_{21}$ from (7) we get.

$$T_{21} = T^m \quad (9)$$

Equation (8) provide us with a very important result. It indicates that, in order to get the trans-admittance (as well as the I/O gains) of a 2-port circuit N, all we need to do is to replace each I/O port with a nullor, as shown in Fig. 3(c), and then find the determinant T^m for the circuit N with the nullor attached. Therefore, there is no need to find the cofactor T_{21}, which traditionally demands applying the 2-tree technique and its long procedures [1]. This is stated in Theorem 3.

Theorem 3: Consider a 2-port linear circuit as shown in Fig. 2(a). To find the cofactor T_{21} in (7) all we need to do is to find the STP of the circuit where a nullor replaces the pair of the I/O ports, as shown in Fig. 3(c).

Evidently, Theorem 3 stands valid for multi-I/O ports circuits as well. To deal with this situation we enumerate the pairs of I/O ports and then assign one nullor to each pair, and proceed as we did for a single 2-port.

Combination of Theorem 2 and Theorem 3 provide a comprehensive and uniformity in circuit analysis, which can be stated as follows. However, before that let us make some definitions.

B. Nullor Circuit

A *nullor circuit* contains passive components and nullors. An *all-nullor circuit* contains all nullors with no passive element. An all-nullor circuit consists of a *nullator network* and a *norator network* combined. Figure 4(a) shows an all-nullor circuit, and Figs. 4(b) and (c) show the corresponding nullator and norator networks separated. Notice that all four nullors in the all-nullor circuit are positive (both arrows are toward the common node).

C. Uniformity

To find a (numerical or symbolic) transfer function of an active linear circuit N, which contains dependent sources, nullors, and I/O ports, we only need to construct a single nullor circuit N_n, as described below.

1. Replace all active devices (VCCS) with nullors.
2. For each pair of an input current source and an output voltage port (I/O) in N remove the input current source and instead add a nullor to the ports, as shown in Fig. 3(c).

So far, we have been able to convert a circuit N with active devices, nullors, and I/O ports into a single nullor circuit N_n. The next step is to apply the AM to N_n and find all the STPs associated with the circuit that leads to the computation of T and T_{21}, and finally to y_{ji}, for all i and j.

So, in brief, an active linear circuit N of any complexity and number of I/O ports can be transformed into a nullor circuit, N_n, where, while the passive parts remain unchanged,

[1]We will take care of the sign later.

each dependent source or an I/O port is replaced with a nullor. Section IV describes how we can find a transfer function in the circuit, either in numerical form or in symbolic form.

IV. Admittance Method for Nullor Circuits

Our objective is now to compute the STPs of a nullor circuit N_n. To achieve this goal, we consider two separate operations. 1) The AM operations applied to the passive components of N_n, and 2) operating on the all-nullor circuit that is resulted from N_n, after we have done with the passive elements. This circuit contains all the nullors. In dealing with the passive circuit, we apply *AM* procedure until we reach to a final 2-terminal component with its admittance $y_p = n_p/d_p$, where $n_p = T_p$ representing the determinant of the passive circuit.

In the second step, we need to find the STP, T_n, of the all-nullor circuit. The final determinant of the original circuit N is then found as

$$T = T_p * T_n \tag{10}$$

Hence, after getting T_p for the passive elements, the problem is how to find T_n. This is stated in Theorem 4.

Theorem 4: The STP of an all-nullor circuit T_n is either 0, 1, or -1.

Proof: First, the magnitude of the STP cannot be greater than 1. This is because each individual nullor has its STP = 0, 1 or -1 (Fig. 2).

Now, given an all-nullor circuit, the problem is then to find rules that indicate whether the STP T_n is 0, 1, or -1. To find that out, we first split the problem into two parts, the magnitude, which is $STP_{mag} = 0$ or 1, and the sign, s (+ or $-$). We will discuss each separately.

Theorem 5: The magnitude, STP_{mag}, of an all-nullor circuit is 1 if and only if each one of the nullator and norator networks (together forming the all-nullor circuit) hform a single tree with no loop. Otherwise, $STP_{mag}, = 0$.

Proof: Because each element in the nullator or norator network represents a VCCS device or an I/O port it must be present in every tree in the STP. Hence, no loop in either nullator or norator network is permissible, and the STP must consist of a single tree, otherwise not all of the nullators (or norators) can be in the same tree.

Corollary 1: An all-nullor circuit has a non-zero STP_{mag}, only if the total number of its nodes is equal to the total number of nullors plus one.

For example, take the case of Fig. 4. The nullator network is a single tree and has no loop but the norator network has one loop. Therefore, the $STP_{mag} = 0$.

Now we should start with the sign of an all-nullor circuit. Algorithm 2 explains the entire process.

For the proof of Algorithm 2, notice that, each time we short circuit a nullor we do short circuit both the nullator and the norator in the positive direction, which it does not change s. Therefore, the sign of s depends on the number of changes we have made in the direction of nullators and norators.

[2]In practice, the number of 4-terminal nullors may exceed three (with no certainty) as long as there are enough 3-terminals to start the process of the short-circuiting until the 4-terminals turn into 3-terminals, Appendix B.

Algorithm 2 To Find the Determinant of an All-Nullor Circuit

1. Given an all-nullor circuit N_n with k nullors, we assume that except for a maximum of three 4-terminals the rest of the nullors are 3-terminals.[2] Next, separate the nullator and norator networks from each other, and begin eliminating nullors one by one starting from the 3-terminals. In case the arrows in both corresponding nullator and norator are not toward or away from the common node change the sign s accordingly. Then short-circuit the nullor elements with the common node removed, and move to the next nullor (see Appendix B).
2. Do step 1 all the way to the last nullor, k. It is shown (Appendix B) that the last, up to three, 4-terminal nullors will change to 3-terminals as well.
3. The final determinant of the all-nullor circuit is then $T_n = s^* STP_{mag}$, where $STP_{mag} = 1$ or 0.

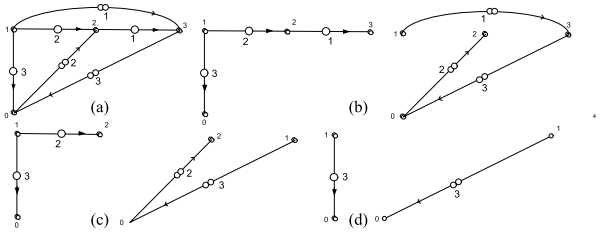


Fig. 5. (a) An all-nullor circuit with the number of nullors k = 3, (b) the nullator and norator networks separated, (c) the nullor 1 is short-circuited, and (d) the nullor 2 is short-circuited, and the nullor 3 is the only one left.

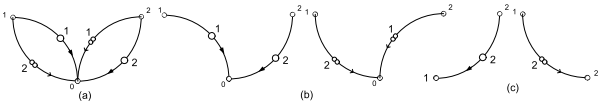


Fig. 6. (a) An all-nullor circuit with the number of nullors k = 2, (b) the nullator and norator networks separated, and (c) the first nullor, 1, is short-circuited, and the nullor 2 is the only one left with $T_n = -1$.

We have three examples to show this. The first one is a three-nullor circuit shown in Fig. 5. According to Algorithm 2, we begin short-circuiting the nullors systematically. As shown in Figs. 5(b), (c), and (d). When we reach to the last nullor, 3, we find its sign to be positive. Therefore, the final $T_n = 1$.

In the second example, we have a two-nullor circuit shown in Fig. 6 (a). Figures 6 (b) and (c) show the two nullator and norator networks separated. Again, we short-circuit the first nullor (i.e., the nullator and norator in the two networks) and will be left with the last nullor, 2. As noticed (Fig. 6 (d)), the nullor sign is negative. So $T_n = -1$.

In the third example, we have a three-nullor circuit shown in Fig. 7 (a), and the separated nullator and norator networks are shown in Fig. 7 (b). Notice that both nullator and norator networks are single trees, and so, the STP must be either 1 or -1. To find the sign, we begin short circuiting nullor 1 in both networks and get the reduced networks as shown in Fig. 7 (c). However, notice that this action has changed the sign of nullor 2 to negative. Therefore, we need to change the direction of an arrow, and this makes $s = -1$.

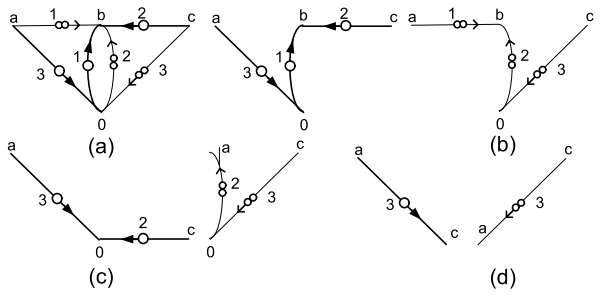


Fig. 7. (a) An all-nullor circuit with the number of nullors k = 3, (b) the nullator and norator networks separated, (c) the nullor 1 is short-circuited, and (d) the nullor 2 is short-circuited, and the nullor 3 is the only one left.

Finally, the networks are further reduced to only one nullor, 3, as shown in Fig. 7 (d). This nullor is negative and requires changing sign, which ultimately makes $s = 1$. Therefore, the final *STP* is $T_n = 1$.

In summary, what we have achieved so far is as follows. For a given active linear circuit N, we first replace all active (VCCS) devices and I/O ports with nullors. This changes N to a totally nullor circuit, N_n. Circuit N_n is then partitioned into a passive circuit and an all-nullor circuit. The passive circuit calculates the magnitude of the *STP*, and the all-nullor circuit provides us with the coefficient 0, 1, or -1 of the final determinant. We have already discussed how to find the coefficient 0, 1, or -1. Therefore, what remains is to calculate the magnitude of the *STP* from the passive portion of N_n, and finally N, which is our next topic.

A. Determinant of the Passive Portion of N_n

As we know, N_n is a nullor circuit with both passive elements and nullors. In applying *AM* operations on the passive circuit, we usually come up with two cases: a passive-passive operation, denoted by *AM-p*, and a passive-nullor operation, denoted by *AM-n*. We have already discussed the *AM-p* in Section II. So, we need to find out about *AM-n*.

Theorem 6 (Parallel/Series Operations in AM-n): If a passive element e_i, with admittances $y_i = n_i/d_i$, is parallel with a nullor element (a nullator or a norator), e_i is removed and d_i is *preserved*. Likewise, if the passive element e_i is in series with a nullor element e_i, the element is short-circuited and n_i is *preserved*. Note that, the *preserved* values, such as d_i and n_i, are the coefficient multipliers forming the *coefficient-multiplier* p, which at the end is multiplied to the final determinant (or the cofactor).

Proof: Suppose the determinant of the original circuit is T. Then in the parallel case, when e_i is removed the determinant becomes $T\{e_i;\ 0\}$. Next, we short circuit e_i and get the determinant $T\{0,\ e_i\} = 0$. This is because by short circuiting e_i we create a nullator or norator self-loop and according to Theorem 5 the STP becomes zero. So, from (4) we are then left with $T = d_i\ T\{e_i;\ 0\}$.

Similarly, in the series case, it is easy to prove that removing e_i produces $T\{e_i;\ 0\} = 0$, and hence by applying (4) we get $T = n_i\ T\{0,\ e_i\}$. This completes the proof.

We are now ready to combine the *AM-p* and *AM-n* operations in a nullor circuit. A brief procedure is given in Algorithm 3, and more details can be found in [10].

Algorithm 3 To Find the Determinant of an Active Circuit

1. Given a nullor circuit N_n, a set of P/S operations[3] is applied to make N_n P/S free.
2. In case N_n is reduced to a 2-terminal passive component e_t with admittance $y_t = n_t/d_t$, then $T_t = s_t p_t n_t$ is the final determinant of N_n, where, p_t is the *coefficient-multiplier*, and s_t is the sign (0, 1, or -1) associated with the all-nullor circuit.
3. In case N_n is not reduced to a 2-terminal passive component, find a node n_i that has the lowest degree,[4] say k. Remove $m = k - 2$ passive elements from n_i to make it a series node, and store the elements removed in a stack. In case there are less than m passive elements incident to n_i, remove all of them and move to another node. When a series node is created, continue applying P/S operations until no more operations is possible. If the circuit is not reduced to a 2-terminal passive component, continue step 3 until a single component is reached.
4. For any element e_j removed from N_n, forming $N_n\{e_j;\ 0\}$, we must connect its corresponding two nodes together to form $N_n\{0;\ e_j\}$. Step 3 operations are again applied to $N_n\{0;\ e_j\}$ to reduce it to a single passive component. Next, use (4) to combine $N_n\{0;\ e_j\}$ and $N_n\{0;\ e_j\}$ and move on. Do the operations multiple times as long as a passive element is left in the stack.
5. Now, we are apparently left with, say q, number of 2-terminal passive components with admittances $y_1 = n_1/d_1$, $y_2 = n_2/d_2, \ldots$ and $y_q = n_q/d_q$, and with their coefficient-multipliers p_1, $p_2, \ldots$ and p_q, and also their signs s_i, for $i = 1, 2, \ldots, q$. The final determinant (STP) of N_n is then given by

$$T = \sum_{i=1}^{q} s_i\, p_i n_i \tag{11}$$

This concludes Algorithm 3, as well as computing the STPs.

V. Admittance Method for Modern Active Devices

In Section IV, we showed that the AM works in any nullor circuit for finding a transfer function, numerically or symbolic. Now the question is, how does the method works with circuits containing modern active devices [22]?

To respond this question, we first need to identify such devices and then model them using nullor circuits. The next stage in the process is to include these devices into the main nullor circuits. Hence, we are back to a nullor circuit again, although larger and with more nullors. First, it looks normal

[3]From now on the operations are referred to both passive-passive and passive–nullor operations.

[4]Node degree here counts both passive and nullor elements.

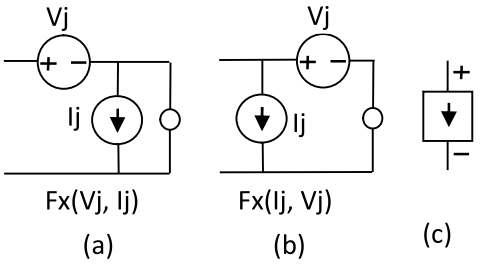


Fig. 8. (a), (b) nullator-based models of a fixator, and (c) denotes a fixator.

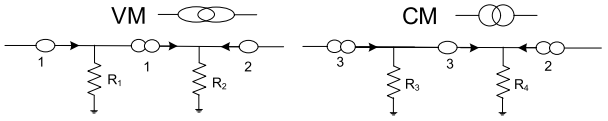


Fig. 9. VM-CM Pair and its nullor model.

and the solution can be achieved by using Algorithm 3 when considering nullors one at a time. The difference, however, is in case of modern devices that each are modeled with more than one nullor. The solution is to deal with all nullors in a device as a whole. The advantage here is that, because of the nullors grouping the computation reduces substantially.

Because of the space limitation, it must be sufficient to work only on some devices such as fixators [26], voltage mirror and current mirror (VM-CM) pairs [27], and a second generation Current Conveyers (CCII+) [28], as examples.

A. Fixators

Fixators are structurally very similar to nullators; instead of having zero voltage and zero current they can accept any arbitrary voltages and currents. Therefore, a fixator can be modeled by a nullator, which is attached to a voltage source and a current source, shown in Fig. 8 [26]. Evidently, a fixator pairing with a norator will form a nullor, and hence, there will be no need to treat them separately.

B. VM-CM

Figure 9 shows a pair of VM-CM along with their nullor models [24], [27], where all resistors are 1. As shown, the model consists of three nullors, which in the AM operation must come as a group of three rather than individual nullors.

Now, as an example let us considered a combined grounded pair of VM-CM, shown in Fig. 10(a) and its nullor model in Fig. 10(b). In checking for Corollary 1, we notice that the circuit has six nodes and three nullors. So, to satisfy Corollary 1 we need to eliminate two nodes. This is done by short-circuiting two resistors and removing (open circuiting) the other two. The actin creates six all-nullor circuits all of which result in having STP = 0, except for one. This case is when we short-circuit r_3 and r_4 and open circuit r_1 and r_2, which provide $STP_{2,4} = r_2 r_4$ in symbolic format, and $STP_{2,4} = 1$ for unit resistances, as shown in Fig. 10(c) [24]. We notice how simple a symbolic representation of a transfer function has been achieved here.

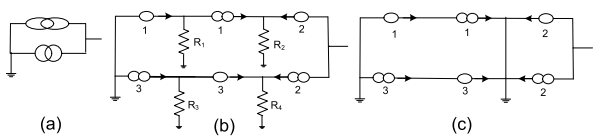


Fig. 10. (a) VM-CM Pair as a device, (b) the nullor circuit, and (c) the all-nullor circuit with non-zero *STP*.

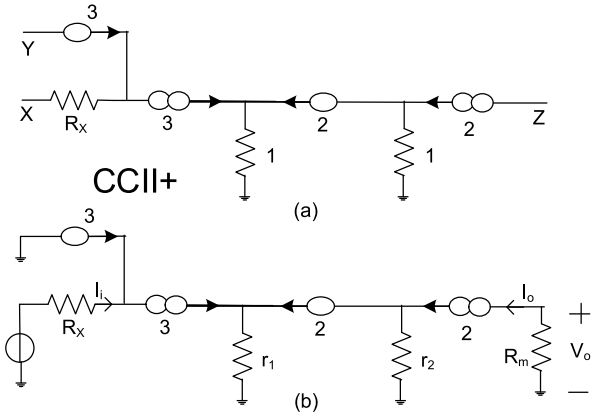


Fig. 11. (a) A nullor model of a CCII+ active device, and (b) a current controlled voltage source – an application.

C. CCII+

Figure 11(a) shows a CCII+ in nullor representation [28]. The model circuit shows two pairs of nullors that must always be treated together. Figure 11(b) shows a CCII+ based constructed trans-impedance amplifier, where

$$Z_m = \frac{V_o}{I_i} = -\frac{r_1}{r_2} R_m \tag{12}$$

Now, to apply the AM procedure we first need to draw the graph representation of the nullor circuit. Figure 12(a) is the graph of the amplifier with the input voltage source removed. In applying, the AM procedure g_x is opened, because it is parallel with a nullor element, and G_m is collapsed, because it is in series with a nullor element (Theorem 6). Similarly, g_2 is opened. Then the nullor circuit left has only g_1 as the passive component. The circuit has four nodes and two nullors. Therefore, according to Corollary 1, for non-zero STP, we need to short circuit g_1. This produced the circuit determinant as $T = g_1\ G_m$.

For computing the trans-conductance Z_m we also need to find the cofactor T_{21}. The circuit graph corresponding to T_{21} is shown in Fig. 12(b), where a nullor is attached to the I/O ports. After we go through a similar AM procedure we come up with $T_{21} = -g_2$. Therefore, we get

$$Z_m = \frac{T_{12}}{T} = \frac{-g_2}{g_1 G_m} = -\frac{r_1}{r_2} R_m \tag{13}$$

which is the same as we found it analytically in (12).

VI. Circuit Examples Using Admittance Method

Now, we are going to run some examples using the AM procedure for conventional circuits.

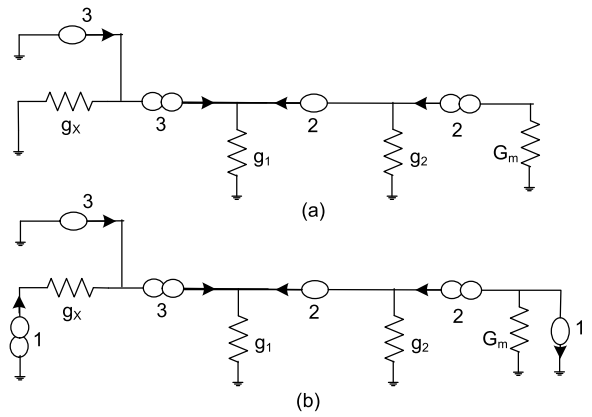


Fig. 12. (a) A nullor model of a CCII+ active device, and (b) a current controlled voltage source – an application.

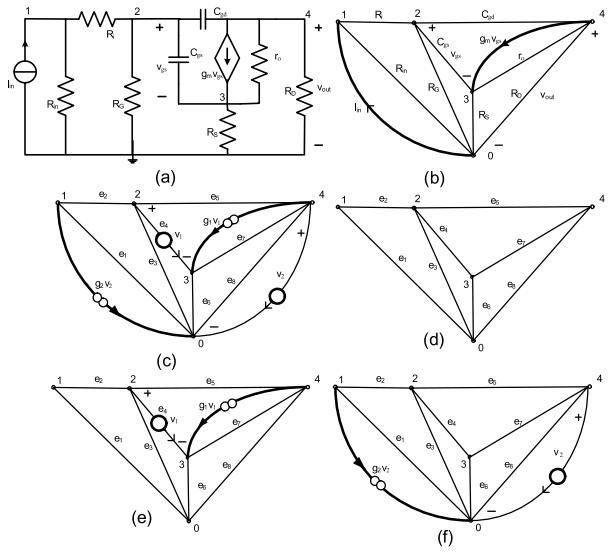


Fig. 13. An MOS amplifier; (a) the linear equivalent circuit for high frequency, (b) graph representation, (c) nullor replacement for active devices and I/O ports, (d) all passive circuit, (e) passive and active, and (f) passive and I/O ports.

Example 1: Consider a single stage MOS amplifier. Figure 13(a) shows the high frequency small signal equivalent circuit of the amplifier, and Fig. 13(b) is the circuit in a graph representation. In Fig. 13(c) we have replaced the active component (VCCS) with a nullor, and we have also removed the input signal and replaced it with another nullor, according to Theorem 2. So, now the circuit has two nullors, g_1 (for the VCCS) and g_2 (for the I/O port). In addition, for simplicity, the components' labels have been changed in Fig. 13(c). Table I shows the list of changes and the component values. However, to make the analysis all resistive, the capacitors C_{gs} and C_{gd} are replace with two resistors 2 KOhms and 50 KOhms, respectively.

Circuit Analysis: According to Theorem 2, there are four determinants related to the NAM of the amplifier circuit that we need to compute. From (6) we can write the STP of the amplifier as

$$T = T^o + g_1 T^1 + g_2 T^2 + g_1 g_2 T^{12} \tag{14}$$

TABLE I
COMPONENT NAMES, LABELS, AND VALUES FOR EXAMPLE 1

Components	*Replacement edges*	*Values*
R_{in}	e_1	*10 KOhms*
R_i	e_2	*2 KOhms*
R_G	e_3	*20 KOhms*
C_{gs}	e_4	*50 pF*
C_{gd}	e_5	*10 pF*
R_S	e_6	*0.2 KOhms*
r_o	e_7	*20 KOhms*
R_o	e_8	*5 KOhms*
g_m	g_1	*5 mA/V*
I/O ports	g_2	*1 mA/V*

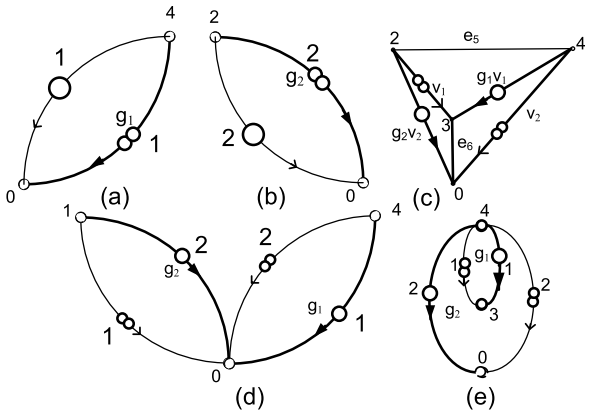


Fig. 14. Processing all-nullor circuits for Example 1.

Basically, the analysis ends up with computing the four determinants (STPs) T^o, T^1, T^2, and T^{12}.

T^o – This is the case when both nullors are removed from the circuit and the circuit is all-passive. The graph representing this case is shown in Fig. 13(d). We apply the *AM* operations on the graph, starting with P/S operations. As it turns out, after nine P/S and one *Partition* (removal and short circuiting e_5) operations the determinant value is found[5] as $T^o = 0.544$.

T^1 – This is the case of the active device (transistor) being in the circuit with $g_1 = g_m$. The graph representing this case is shown in Fig. 13(e). Again, we apply the *AM* operations to the circuit and after ten P/S and one *Partition* operations the graph is reduced to a single nullor, as shown in Fig. 14(a). As we can see, the STP = 1 here. Hence the final determinant becomes $g_1 T^1 = 0.4$, for $g_1 = 5$ mA/V.

T^2 – For this case we need to remove the active source g_m and add the nullor g_2 representing the I/O ports. This is shown in graph of Fig. 13(f). We apply the *AM* operations and after nine P/S and one *Partition* operations the graph is

[5]The simulation program CASD is used here and for later computations.

TABLE II
STEPS TAKEN IN THE *AM* OPERATIONS IN EXAMPLE 1

STP	*Reduction*	Value	Note
T^v	e_5 O	0.42432	e_5 Open
T^v	e_5 S	0.11968	e_5 Short
g_1T^1	e_5 O	0.312	
g_1T^1	e_5 S	0.088	
g_2T^2	e_5 O	0.018	
g_2T^2	e_5 S	0.05	
$g_1\,g_2T^{12}$	e_5 O, e_6 S	-10.0	
$g_1\,g_2T^{12}$	e_5 S, e_6 O	0.05	
T_{main}		0.944	$T^v + g_1T^1$
T_{41}		-12.382	$g_2T^2 + g_1\,g_2T^{12}$

reduced to a single nullor shown in Fig. 14(b). The nullor is also positive here with STP $= 1$. Then the final determinant becomes $g_2T^2 = 0.068$, for $g_2 = 1$ mA/V.

T^{12} – The case is when we allow both nullors, associated with g_1 and g_2, remain in the circuit. The graph for this case is shown in Fig. 13(c). Again, after applying the AM operations the graph is reduced to the one in Fig. 14(c). We notice that, this nullor circuit has four nodes and two nullors. So, according to Corollary 1 one passive element must be short-circuited and the other one open circuited. So we have two cases. We first short-circuit e_6 and open circuit e_5. This generates the all-nullor circuit shown in Fig. 14(d) with STP $= -1$. After including the passive parts and the coefficients g_1, we get $g_1g_2T^{12} = -10.0$. Similarly, we short-circuit e_5 and open circuit e_6 this time. The graph associated with this case is given in Fig 14(e). This case produces STP $= 1$, and after including the passive parts and the coefficients we get $g_1\ g_2T^{12} = 0.05$.

A detailed list of the steps taken in the *AM* operations are given in Table II. For simplicity, the parallel and series operations are dismissed here and the *Partition* operations are only displayed.

Finally, a similar procedure is conducted to find the cofactor T_{11} for the input port. This is done by short circuiting the input port.[6] The resulted value is found to be $T_{11} = 2.655$. With the three values $T = T_{main}$, T_{41}, and T_{11} found, we are now able to calculate the amplifier gain, the input impedance, and the trans-impedance as:

$$A_v = T_{41}/T_{11} = -12.382/2.655 = -4.66365\ V/V$$
$$R_{in} = T_{11}/T = 2.655/0.944 = 2.655\ KOhms$$
$$R_m = T_{41}/T = -12.382/0.944 = -13.11365\ KOhms$$

The results are also checked with SPICE simulation, which gives us the same responses.

Programming: A computer program in C++, called Circuit Analysis, Simulation and Design (CASD), is developed for finding the transfer functions in linear active circuits using the proposed method. CASD produces the NAM determinants and cofactors from which we get the input impedance, gain and any other circuit transfer functions. The program is coded in such a way that it can also produce the circuit parameters in symbolic format. However, the program is still not commercialized for general use, pending for some possible publications and refinements. A sample screen shot of the CASD program results is shown in Fig. 15.

[6]The procedure is not reported here for brevity.

```
!!!!!!!!!!!!!!!! Start cpy(), in sub !!!!!!!!!!!!!

dt[0] = 0.544
dt[1] = 0.4
dt[2] = 0.068
dt[3] = -12.45
dt[4] = 0

Final results:
              Tmain = 0.944
              T21[0] = -12.382
              z21 = -13.1165

END 4/6/2021, Main Program!, actval = 1/1
```

Fig. 15. A sample screen shot of the CASD program for Example 1.

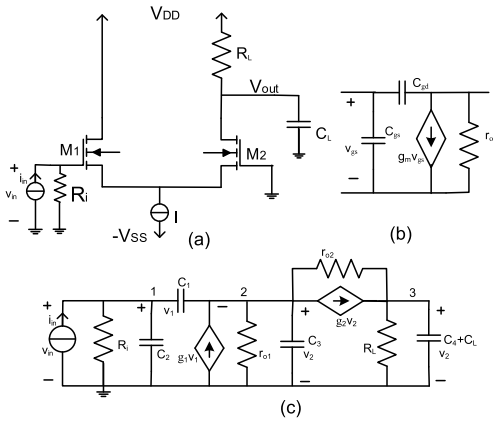


Fig. 16. (a) An nMOS differential pair, (b) the high frequency model of the transistor, and (c) the linearized amplifier circuit.

Example 2: We take an nMOS differential pair for this example [10]. The actual amplifier, the high frequency model of the transistor, and the linearized amplifier circuit are given in Figs. 16(a), (b), and (c).

For the convenience, the linear amplifier circuit is also given in graph representation in Fig. 17(a) with the circuit elements renamed, given in Table III.

Next, we apply the *AM* operations to the main circuit, Fig. 17(a), by going through Algorithm 1. We realize that there are three pairs of parallel elements, which after applying P/S operations they are reduced to e_a, e_b, and e_c, with the admittances $y_a = y_1||y_3$, $y_b = y_6||y_7$, and $y_c = y_4||y_5$, where, $||$ denotes parallel operation. Figure 17(b) shows the new graph after the P/S operations are done. Next, according to Algorithms 1 and 3, we get the graphs for N^o, N_1^m, N_2^m, N_3^m, N_{12}^m, N_{13}^m, N_{23}^m, and N_{123}^m, shown in Figs. 17(c) to (h). Graphs for N_{13}^m and N_{23}^m are missing purposely. We notice that the circuit N^o is a P/S circuit and its determinant T^o is obtained by doing two series operations following by two parallel operations. This is shown below, with * indicating the series operation.

$$y_d = y_8\ ^*\ y_b, \quad y_e = y_c||y_d, \quad y_f = y_2 * y_e, \quad \text{and}$$
$$y_g = y_a||y_f. \tag{15}$$

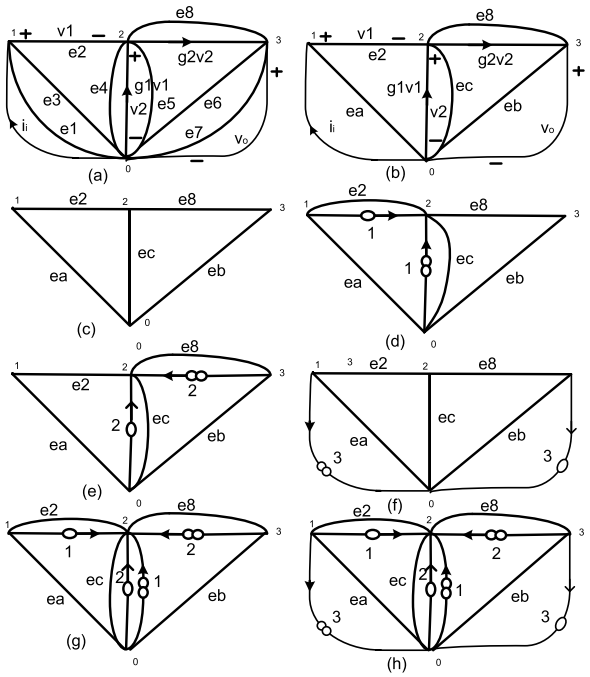


Fig. 17. (a) Graph representation of the linear amplifier circuit; (b) The same circuit with the input signal removed, and Step 1 in Algorithm 1 applied; (c) the passive circuit N^o; (d) the active circuit N_1^m; (e) the active circuit N_2^m; (f) the active circuit N_3^m (g) the active circuit $N_{1,2}^m$; (h) the active circuit $N_{1,2,3}^m$.

Ultimately, the circuit is reduced to a single element e_g with the admittance y_g. Now, if we symbolically expand y_g and write it in terms of s we get $y_g(s)$, also as the input admittance of the amplifier with $g_1 = g_2 = 0$ as

$$y_{in}^o = y_g = \frac{T^0}{T_{1,1}^0} = \frac{6 * 10^3}{12 * 10^2} * \frac{12s^3 + 82s^2 + 87s + 20}{3s^2 + 4s + 1} \ \mu A/V \tag{16}$$

where, the conductances are in $\mu A/V$, the capacitors in fF, and the frequencies in GHz. Also note that, because there is no division involved in computing determinants, the coefficient 6000/1200 remains as a ratio in (16).

Likewise, we get the passive portion of the voltage gain $A_{vo} = v_{out}/v_{in}$ as

$$\frac{v_{out}^0}{v_{in}} = \frac{T_{1,2}^0}{T_{1,1}^0} = \frac{600}{1200} * \frac{s}{3s^2 + 4s + 1} \ V/V \tag{17}$$

It is interesting to note that, because A_{vo} is the gain when all active devices are removed, the voltage gain is less than 1 for any value of s. Specifically, when s = 0 the gain becomes zero, as expected. This is evident, because C_2 for DC opens the feedback between the input and the output ports of the amplifier.

Active – g_1, g_2, $g_3 \ldots$: Next, we continue with the circuits that contain active devices plus the I/O ports, individually and in combinations.

g_1 – The graph of the amplifier, with only g_1 present, is shown in Fig. 17(d). The circuit is again a P/S circuit. After applying P/S operations the circuit reduces to a single nullor with the STP = 1. Here is the sequence of the operations:

TABLE III
COMPONENT NAMES, LABELS, AND VALUES FOR EXAMPLE 2

Components	*Replacement edges*	*Values*
R_i	e_1	*10 KOhms*
C_1	e_2	*30 fF*
C_2	e_3	*5 fF*
r_{o1}	e_4	*50 KOhms*
C_3	e_5	*30 fF*
R_L	e_6	*50 KOhms*
$C_4 + C_L$	e_7	*60 fF*
r_{o2}	e_8	*50 KOhms*
g_1	g_1	*5 mA/V*
g_2	g_2	*5 mA/V*
I/O ports	g_3	

The element e_c in parallel with the norator is removed with no effect on the STP. The element e_a with $y_a = n_a/1$ is in series with the nullator. Short circuitting e_a multiplies the STP by n_a (Theorem 6). This generates a single nullor with the STP = 1. Finally, the elments e_8 and e_b become parallel, creating a single element e_d with $y_d = n_d/d_d$. So, the circuit determinant is $T_1^m = n_d$, which in expanded form become

$$T_1^m = y_a * (y_b || y_8) = 100(3s^2 + 62s + 40) \tag{18}$$

g_2- The circuit graph is shown in Fig. 17(e), which is also a P/S circuit. We follow the same rout as we did for g_1.

The element e_c in parallel with the nullator is removed, and the element e_8 in parallel with the norator is also removed. The element e_b is in series with the norator. Short circuitting e_b multiplies the STP by n_b. This generates a single nullor with the STP = 1. Finally, the elments e_2 and e_a become parallel creating a single element e_d. So, the circuit determinant is $T_2^m = n_d$, which in expanded form become

$$T_2^m = y_b \ ^* \ (y_a || y_2) = 100(21s^2 + 67s + 20) \tag{19}$$

g_3- The circuit graph is shown in Fig. 17(f), and the STP can be simply found as.

$$T_3^m = y_2 \ ^* \ y_8 = 600s \tag{20}$$

g_1g_2- The circuit graph for g_1g_2 is shown in Fig. 12(g), and it is a P/S circuit. However, the resulted graph ends up with two nullors, one series and one parallel. Both nullors have negative signs. The parallel nullor makes the STP = −1, but the series one produces the STP = 0. Therefore, $T_{1,2}^m = 0$.

g_1g_3– A similar analysis will reduce the associated graph (not shown) to a single element e_8, and with the STP = 1 for the all-nullor circuit we get $T_{1,3}^m = 20$.

g_2g_3– The graph (not shown) for this case is also reduced to a single element e_2, and with the STP = 1 for the all-nullor circuit we get $T_{2,3}^m = 30s$.

$g_1g_2g_3-$ The circuit graph representing this case is shown in Fig. 17(h). There are five passive elements e_2, e_8, e_a, e_b, and e_c in the graph, and all five are parallel with nullors' elements. Thus, we can simply remove then all with no effect on the determinant (Theorem 6, and $d_i = 1$). We are now left with an all-nullors, as shown in Fig. 7(a). Therefore, as we investigated previously, the $STP = T^m_{1,2,3} = 1$.

Finally, we are prepared to get the circuit transfer functions such as the gains, input impedance and transfer impedance. The approach makes it possible to write the functions in symbolic forms, both in terms of g_m and s. We begin by writing the circuit determinant T, and the cofactors T_{21} and T_{11}.

$$T = T^0 + g_1T^m_1 + g_2T^m_2 + g_1g_2T^m_{12} \tag{21}$$

$$T_{2,1} = g_3T^m_3 + g_1g_3T^m_{13} + g_2g_3T^m_{23} + g_1g_2g_3T^m_{123} \tag{22}$$

After replacing the values, we get

$$T = 100 * [720s^3 + (4920 + 3g_1 + 21g_2)s^2 + (5220 + 62g_1 + 67g_2)s + 1200 + 40g_1 + 20g_2] \tag{23}$$

Similarly, we get

$$T_{2,1} = 30 * (20 + g_2)s + (20 + g_2)g_1 \tag{24}$$

$$T_{1,1} = 3600s^2 + (4800 + 60g_1 + 60g_2)s + 1200 + 40g_1 + 20g_2 \tag{25}$$

So, we can simply replace for T, T_{21}, and T_{11} to write the input impedance, the voltage gain, and the transfer impedance as

$$z_{in} = \frac{T_{1,1}}{T} \tag{26}$$

$$A_v = \frac{T_{2,1}}{T_{1,1}} \tag{27}$$

$$z_m = \frac{T_{2,1}}{T} \tag{28}$$

This concludes our Example 2.

A. Comparing the AM With Others Methods Reported

Now, we need to discuss about the claims made in this presentation, i.e., why the presented procedure, both the *AM* technique and the nullor methodology, are advantageous compare with other reported techniques? The major portion of this comparison is given in Section I, Introduction. The fundamental message here, however, is the following: *No matter how much complex and involved is a linear active circuit, the use of the Tree Enumeration Method (TEM) is limited to the passive portion of the circuit plus the use of an all-nullor circuit that specifies the sign*. This major achievement categorically removes any other requirements such as two-graphs and 2-trees that have been essential parts of most reported methods in dealing with *TEM*.

The keys to this simplicity are two. First, the ability to replace active (VCCS) devices as well as I/O ports with nullors. Second, the use of *AM*, which is basically a simple sequence of parallel and series (P/S) operations that systemically reduces a circuit to a single element, where, it represents the determinant or a cofactor of the NAM of the circuit, or the reduced circuit reaches to an all-nullor circuit. It is shown that the P/S operations shrink the passive portion of the circuit quickly and accurately to a final element. This is especially true for large and sparser circuits, where finding a set of P/S operations is a matter of search or removal of a few elements. Although in many cases the circuits are *P/S circuits* (simply reduced to a single element through a series of P/S operations), in more complex cases the removal of one or more elements will smoothly resume the P/S operations. Another property of the *AM* is the absence of the division in the operations, as there is no division involved in finding determinants. Finally, it is important to note that, because of the systematic reduction of the circuit, the *AM* is ideal for symbolic representation of transfer functions.

VII. Conclusion

The purpose in this presentation is to develop a uniform and comprehensive procedure for symbolic analysis of linear active circuits using the tree enumeration techniques such as the Sum of the Tree Products (STP) of the circuit. We have achieved our objective in two stages. In the first stage a circuit with active devices (VCCSs), and I/O ports, is converted to a nullor circuit, i.e., to a circuit with no active devices but only passive components and nullors. For further simplification, the nullor circuit is also partitioned into two distinct parts, a passive circuit and an all-nullor circuit. We have shown that the magnitude of the determinant of the NAM of the circuit is the same as the STP (determinant) of the passive part. Whereas, the sign (0, 1, or -1) of the STP comes from its all-nullor circuit.

The other unique development in this presentation is the replacement of the normal STP methodology, based on the tree enumeration, with an advanced *Admittance Method* (*AM*) procedure. As we have shown, by applying the *AM* procedure the entire two-graph theory for active circuits as well as the use of 2-tree techniques for I/O ports analysis are eliminated. Overall, the new developments substantially simplifies the circuit analysis and makes it quite efficient for symbolic representation of transfer functions, so that it might present itself as a viable alternative to numerical algorithms, particularly for well sparse circuits.

Finally, a computer program in C++, called Circuit Analysis, Simulation and Design (CASD), is developed for the project. CASD produces the NAM determinants and any transfer functions of circuits with VCCS and multiple I/O ports. The extension of the program is underway to cover circuits with other kinds of active devices, namely VCVS, CCVS, and CCCS, in preparing the transfer functions of the circuit in symbolic format.

Appendix A
Efficient Programming

One of the draw backs in the *AM* operations, like any other Tree Enumeration Method in general, is that when the circuit is partitioned the same *AM* operations may get repeated

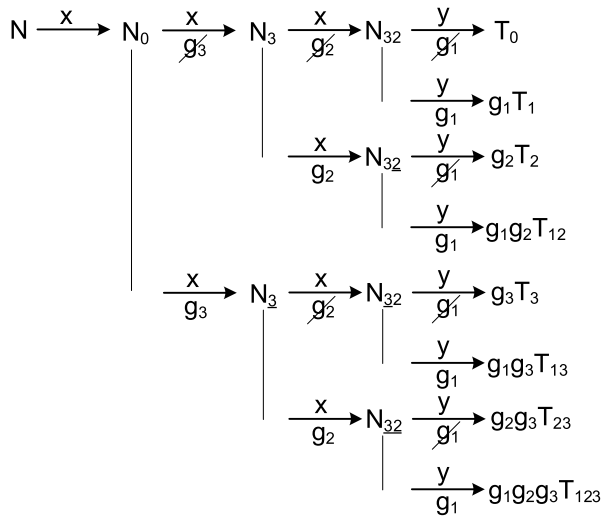


Fig. 18. Flow diagram for finding determinants and cofactors of a NAM. x and y both specify exhaustive P/S operations. However, in x no passive element that is in parallel or in series with a nullor element is removed. $\not{g_i}$ denotes the removal of g_i from the circuit.

Algorithm 4 Efficient Programming to Find the Circuit Determinant

1. Apply the P/S operations to reduce a circuit N to a P/S free circuit N_o. Store N_o in a stack. Next, remove the active component g_3 and apply the P/S operations to N_o to reduce it to a P/S free circuit N_3. Store N_3 in the stack. Continue the process until no active device remains in the circuit and the circuit is all-passive. Apply *AM* operations to the circuit to reduce it to a single element with the determinant T_o.
2. Now, get the last item N_{32} stored in the stack out and apply the P/S operations to reduce it to a single element. However, because the circuit N_{32} did contain g_1 the determinant becomes g_1T_1.
3. Next, move one-step back and get N_3 out of the stack and move on as discussed in 1. As it is shown in Fig. 18, the operation ends up getting g_2T_2. Similar procedures will result in computing $g_1g_2T_{12}$, g_3T_3, $g_1g_3T_{13}$, $g_2g_3T_{13}$, and $g_1g_2g_3T_{123}$.
4. Finally, all the terms so computed are added up together in (6) to obtain the determinant or a cofactor of the circuit NAM.

for different parts. This evidently increases the computational overhead, reducing the effectiveness of the method.

One way to reduce this difficulty is to establish a hierarchical structure for reducing the circuit to a final single element.

The following procedure is given for a linear active circuit N that has three active (VCCS) components (or alternatively, two VCCSs and one I/O ports). The method is certainly applicable to circuits with more devices and multiple I/O ports. A flow diagram of the entire *AM* operations, in steps, is demonstrated in Fig. 18, and the procedure is explained in Algorithm 4.

APPENDIX B

A. Dealing With 4-Terminal Devices

As stated in Section II, determining signs for 4-terminal devices such as VCCSs and nullors is not simple. In Section II we broke a 4-terminal VCCS into two 3-terminal devices and solved the sign problem. However, this increase the number of active devices; hence, more computation is required. The fact that the AM process removes the entire passive elements in the circuit and at the end only an all-nullor circuit remains is a great achievement. This means that, if the passive elements in the circuit are eliminated (short circuited) the chances are that some of the 4-terminal devices become 3-terminal or even 2-terminal devices. In addition, it is shown that, in any circuit, if there are three or less number of 4-terminal nullors, they will eventually convert to 3-terminals when we reach to the final all- nullor circuit. So, in conclusion, at least three 4-terminal nullors (devices) are permissible in a nullor circuit.

B. Circuits With Three or Less 4-Terminal Devices

Let us assume that a circuit N, after all its active devices and I/O ports are replace with nullors, is reduced to an all-nullor circuit N_n. Further, let us assume that N_n contains n nullors, three of which are 4-terminals. Now, in order to find the sign (0, 1, or -1) of N_n we need to use Algorithm 2. However, in ordering the nullors for the process in Step 2, we start with the 3-terminals and then go to the 4-terminals only when the 3-terminals are all exhausted. So, basically, for the all-nullor circuit that remains we have nullators and norators trees, each having three branches. With all possible combinations of the branches it is simple to see that at least one nullor comes up with 3-terminal, and the rest will follow suite. This is stated in Theorem 1B.

Theorem 1B: The sign of the STP of any active circuit N is determined if its all-nullor circuit N_n does not have more than three 4-terminal nullors.

In conclusion, the process of sign determination for cofactors can be extended to include circuits with up to three 4-terminal active devices or I/Os.

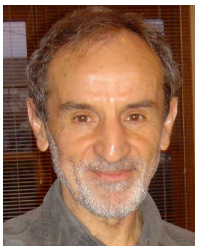
C. 3-Terminal Nullors With Shared Common Node

In some rare cases we may end up with an all-nullor circuit that contains two or more nullors in a group that share their common nodes. The problem with this case is that, when we short-circuit the elements of a nullor in the group the common node disappears, leaving the other nullors in the group 4-terminals. An ad hoc solution to the problem is to leave such cases to the end of the process. The chances are that they turn into 3-terminals, as discussed earlier in this Appendix.

REFERENCES

[1] P. M. Lin, *Symbolic Network Analysis*. New York, NY, USA: Elsevier, 1991.
[2] S. Seshu and M. B. Reed, *Linear Graphs and Electrical Networks*. Reading, MA, USA: Addison-Wesley, 1961.
[3] G. Shi, S. X.-D. Tan, and E. Tlelo-Cuautle, *Advanced Symbolic Analysis for VLSI Systems*. New York, NY, USA: Springer, Jul. 2014, doi: 10.1007/978-1-4939-1103-5.

[4] R. Giomi and A. Luchetta, "Enhanced two-graph theory for symbolic analysis of electrical networks," in *Proc. 3rd Int. Workshop Design Mixed-Mode Integr. Circuits Appl.*, Jul. 1999, pp. 44–47.
[5] R. Hashemian and M. S. Bakhtiar, "Generation of all possible trees of a graph in independent groups," *Comput.-Aided Des.*, vol. 7, no. 3, pp. 157–159, Jul. 1975.
[6] R. Hashemian, "An algorithm for direct evaluation of network transfer functions," *Comput.-Aided Des.*, vol. 8, no. 4, pp. 264–266, Oct. 1976.
[7] M. Fakhfakh, E. Tlelo-Cuautle, and F. V. Fernandez, *Design of Analog Circuits Through Symbolic Analysis*. Sharjah, United Arab Emirates: Benthone Books, 2012.
[8] E. Tlelo-Cuautle and C. Sanchez-Lopez, *Symbolic Analysis of Analog Circuits Containing Voltage Mirrors*. Cham, Switzerland: Springer, 2010.
[9] M. Pierzchala and M. Fakhfakh, "Symbolic analysis of nullor-based circuits with the two-graph technique," *Circuits, Syst., Signal Process.*, vol. 33, no. 4, pp. 1053–1066, Apr. 2014.
[10] R. Hashemian, "Application of nullors in symbolic single port transfer functions using admittance method," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.
[11] A. D. Grasso, D. Marano, S. Pennisi, and G. Vazzana, "Symbolic factorization methodology for multistage amplifier transfer functions," *Int. J. Circuit Theory Appl.*, vol. 44, no. 1, pp. 38–59, Jan. 2016.
[12] M. Fakhfakh and M. Pierzchala, "Computing symbolic transfer functions of CC-based circuits using Coates flow-graph," in *Proc. 5th Int. Conf. Design Technol. Integr. Syst. Nanosc. Era*, Mar. 2010, pp. 1–4.
[13] C. Sanchez-Lopez, F. V. Fernandez, E. Tlelo-Cuautle, and S. X.-D. Tan, "Pathological element-based active device models and their application to symbolic analysis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 6, pp. 1382–1395, Jun. 2011.
[14] C. Sánchez-López, E. Martínez-Romero, and E. Tlelo-Cuautle, "Symbolic analysis of OTRAs-based circuits," *J. Appl. Res. Technol.*, vol. 9, no. 1, pp. 69–80, Apr. 2011.
[15] I. Asenova and F. Balik, "Multiparameter symbolic sensitivity analysis of active circuits by using nullor model and modified Coates flow graph," in *Proc. ELEKTRO*, May 2012, pp. 401–406.
[16] S. Hamedi-Hagh, "Characterization of active inductors with modified determinant expansion analysis," in *Proc. IEEE Dallas Circuits Syst. Conf. (DCAS)*, Oct. 2016, pp. 1–4.
[17] R. Hashemian, "Symbolic representation of network transfer functions using norator–nullator pairs," *IEE J. Electron. Circuits Syst.*, vol. 1, no. 6, p. 193, 1977.
[18] J. Braun, "Topological analysis of networks containing nullators and norators," *Electron. Lett.*, vol. 2, no. 11, pp. 427–428, Nov. 1966.
[19] M. E. Parten and R. H. Seacat, "Topological analysis of networks containing nullators and norators using residual networks," in *Proc. 23th Annu. Southwestern IEEE Conf. Exhib.*, Houston, TX, USA, Apr. 1971, pp. 39–42.
[20] J. Hoekstra, "Nullor-based circuits for quantum technology," *Int. J. Circuit Theory Appl.*, vol. 45, no. 7, pp. 1001–1016, Jul. 2017, doi: 10.1002/cta.2352.
[21] S. D. Djordjević, P. M. Petković, and V. B. Litovski, "A new topology oriented method for symbolic analysis of electronic circuits," *J. Circuits, Syst. Comput.*, vol. 19, no. 8, pp. 1781–1795, Dec. 2010.
[22] S. Lasota, "Models of modern active devices for effective and always cancelation-free symbolic analysis," *IFAC-PapersOnLine*, vol. 49, no. 25, pp. 80–85, 2016.
[23] S. Lasota, "Symbolic analysis of electric networks with higher order summative cofactors and parameter decision diagrams," *Int. J. Circuit Theory Appl.*, vol. 46, no. 10, pp. 1796–1826, Oct. 2018.
[24] V. Filaretov and K. Gorshkov, "Efficient generation of compact symbolic network functions in a nested rational form," *Int. J. Circuit Theory Appl.*, vol. 48, no. 7, pp. 1032–1056, 2020.
[25] R. Hashemian, "A comprehensive nodal/branch circuit analysis including fixator–norator pairs in analog circuits," in *Proc. IEEE 61st Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2018, pp. 125–128.
[26] R. Hashemian, "Application of fixator–norator pairs in designing active loads and current mirrors in analog integrated circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 12, pp. 2220–2231, Dec. 2012.
[27] C. Sanchez-Lopez, "Pathological equivalents of fully-differential active devices for symbolic nodal analysis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 3, pp. 603–615, Mar. 2013.
[28] E. Tlelo-Cuautle, C. Sanchez-Lopez, and D. Moro-Frıas, "Symbolic analysis of (MO)(I) CCI (II)(III)-based analog circuits," *Int. J. Circuit Theory Appl.*, vol. 38, no. 6, pp. 649–659, 2010.



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